x5

EXTRA TOPICS RELATED TO

Internal Op Amp Circuits

This supplement contains material removed from previous editions of the textbook. These topics continue to be relevant and for this reason will be of great value to many instructors and students.

The topics presented here relate to Chapter 13 of the eighth edition. In particular, the 741 op-amp circuit is analyzed in full detail. The final section explains special requirements of BJT op amps designed for low supply voltages.

x5.1 The 741 Circuit

Figure x5.1 shows the 741 op-amp circuit. In keeping with the IC design philosophy, the circuit uses a large number of transistors, but relatively few resistors and only one capacitor. This philosophy is dictated by the economics (silicon area, ease of fabrication, quality of realizable components) of the fabrication of active and passive components in IC form (see Section 8.1 and Appendix A).

As in the case of most general-purpose IC op amps, the 741 requires two power supplies, $+V_{CC}$ and $-V_{EE}$. Normally, $V_{CC} = V_{EE} = 15$ V, but the circuit also operates satisfactorily with the power supplies reduced to much lower values (such as ±5 V). It is important to observe that no circuit node is connected to ground, the common terminal of the two supplies.

With a relatively large circuit like that shown in Fig. x5.1, the first step in the analysis is to identify its recognizable parts and their functions. Thus, we begin with a qualitative description of the circuit. Our description is aided by the division of the circuit into its various parts, as indicated in the diagram.

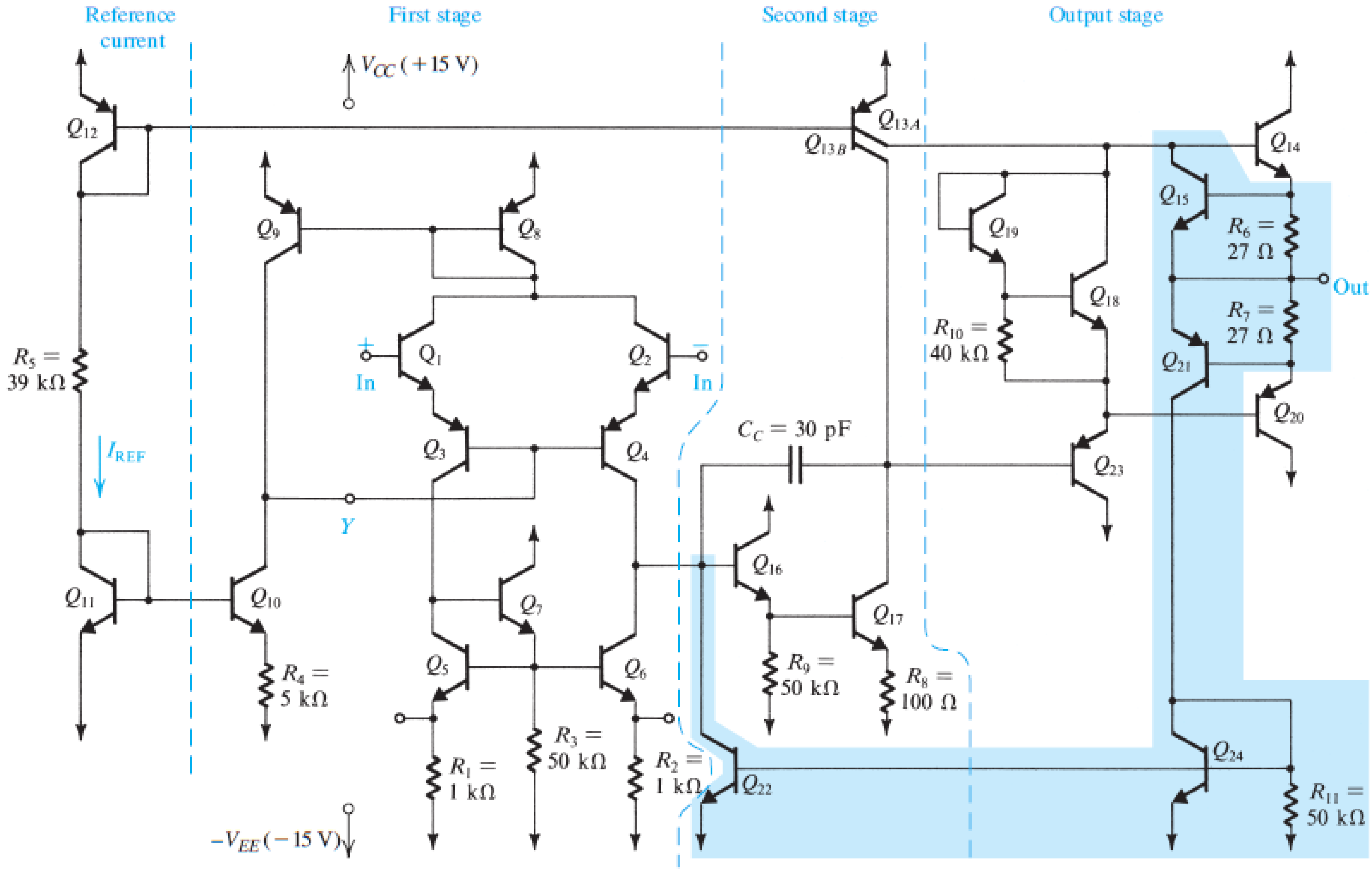

Figure x5.1 The 741 op-amp circuit: Q_{11}, Q_{12}, and R_5 generate a reference bias current, I_{REF}. Q_{10}, Q_9, and Q_8 bias the input stage, which is composed of Q_1 to Q_7. The second gain stage is composed of Q_{16} and Q_{17} with Q_{13B} acting as active load. The class AB output stage is formed by Q_{14} and Q_{20} with biasing devices Q_{13A}, Q_{18}, and Q_{19}, and an input buffer Q_{23}. Transistors Q_{15}, Q_{21}, Q_{24}, and Q_{22} serve to protect the amplifier against output short circuits and are normally cut off.

Bias Circuit The reference bias current of the 741 circuit, I_{REF}, is generated in the branch at the extreme left of Fig. x5.1, consisting of the two diode-connected transistors Q_{11} and Q_{12} and the resistance R_5. Using a Widlar current source formed by Q_{11}, Q_{10}, and R_4, bias current for the first stage is generated in the collector of Q_{10}. Another current mirror formed by Q_8 and Q_9 takes part in biasing the first stage.

The reference bias current I_{REF} is used to provide two proportional currents in the collectors of Q_{13}. This double-collector lateral *pnp* transistor can be thought of as two transistors whose base–emitter junctions are connected in parallel. Thus Q_{12} and Q_{13} form a two-output current mirror: One output, the collector of Q_{13B}, provides bias current and acts as a current-source load for Q_{17}, and the other output, the collector of Q_{13A}, provides bias current for the output stage of the op amp.

Two more transistors, Q_{18} and Q_{19}, take part in the dc bias process. The purpose of Q_{18} and Q_{19} is to establish two V_{BE} drops between the bases of the output transistors Q_{14} and Q_{20}.

Short-Circuit-Protection Circuitry The 741 circuit includes a number of transistors that are normally off and conduct only if one attempts to draw a large current from the op-amp output terminal. This happens, for example, if the output terminal is short-circuited to one of the two supplies. The short-circuit-protection network (shown in color in Fig. x5.1) consists of R_6, R_7, Q_{15}, Q_{21}, Q_{24}, R_{11}, and Q_{22}. In the following we shall assume that these transistors are off. Operation of the short-circuit-protection network will be explained in Section x5.1.3 of this supplement.

The Input Stage The 741 circuit consists of three stages: an input differential stage, an intermediate single-ended high-gain stage, and an output-buffering stage. The input stage consists of transistors Q_1 through Q_7, with biasing performed by Q_8, Q_9, and Q_{10}. Transistors Q_1 and Q_2 act as emitter followers, causing the input resistance to be high and delivering the differential input signal to the differential common-base amplifier formed by Q_3 and Q_4. Thus the input stage is the differential version of the common-collector, common-base configuration discussed in Section x3.3 of the extra topics.

Transistors Q_5, Q_6, and Q_7 and resistors R_1, R_2, and R_3 form the load circuit of the input stage. This is an elaborate current-mirror-load circuit, which we will analyze in Section x5.1.3 of this supplement. The circuit is based on the base-current-compensated mirror studied in Section 8.2.4, but it includes two emitter-degeneration resistors R_1 and R_2, and a large resistor R_3 in the emitter of Q_7. As is the case with current-mirror loads, this circuit not only provides a high-resistance load for Q_4 but also converts the signal from differential to single-ended form with no loss in gain or common-mode rejection. The output of the input stage is taken single-endedly at the collector of Q_4.

Every op-amp circuit includes a *level shifter* whose function is to shift the dc level of the signal so that the signal at the op-amp output can swing positive and negative. In the 741, level shifting is done in the first stage using the lateral *pnp* transistors Q_3 and Q_4. Although lateral *pnp* transistors have poor high-frequency performance, their use in the common-base configuration (which is known to have good high-frequency response) does not seriously impair the op-amp frequency response.

The use of the lateral *pnp* transistors Q_3 and Q_4 in the first stage results in an added advantage: protection of the input-stage transistors Q_1 and Q_2 against emitter–base junction breakdown. Since the emitter–base junction of an *npn* transistor breaks down at about 7 V of reverse bias (see Section 6.4.1 of the textbook), regular *npn* differential stages suffer such a breakdown if, say, the supply voltage is accidentally connected between the input terminals. Lateral *pnp* transistors, however, have high emitter–base breakdown voltages (about 50 V), and because they are connected in series with Q_1 and Q_2, they provide protection of the 741 input transistors, Q_1 and Q_2.

Finally, note that except for using input buffer transistors, the 741 input stage is essentially a current-mirror-loaded differential amplifier. It is quite similar to the input stage of the CMOS amplifier in Fig. 13.1.

The Second Stage The second or intermediate stage is composed of Q_{16}, Q_{17}, Q_{13B}, and the two resistors R_8 and R_9. Transistor Q_{16} acts as an emitter follower, thus giving the second stage a high input resistance. This minimizes the loading on the input stage and avoids loss of gain. Also, adding Q_{16} with its 50-kΩ emitter resistance (which is similar to Q_7 and R_3) increases the symmetry of the first stage and thus improves its CMRR. Transistor Q_{17} acts as a common-emitter amplifier with a 100-Ω resistor in the emitter. Its load is composed of the high output resistance of the *pnp* current source Q_{13B} in parallel with the input resistance of the output stage (seen looking into the base of Q_{23}). Using a transistor current source as a load resistance (*active load*) enables one to obtain high gain without resorting to the use of large resistances, which would occupy a large chip area and require large power-supply voltages.

The output of the second stage is taken at the collector of Q_{17}. Capacitor C_C is connected in the feedback path of the second stage to provide frequency compensation using the Miller compensation technique studied in Section 11.10.3 of the textbook. In Section x5.1.4 of this supplement we will see that the relatively small capacitor C_C gives the 741 a dominant pole at about 4 Hz. Furthermore, pole splitting causes other poles to be shifted to much higher frequencies, giving the op amp a uniform –20-dB/decade gain rolloff with a unity-gain bandwidth of about 1 MHz. Note that although C_C is small in value, the chip area that it occupies is about 13 times that of a standard *npn* transistor!

THE CREATOR OF THE µA741: DAVID FULLAGAR

David Fullagar was at Fairchild Semiconductor in 1967 when he designed the µA741, perhaps the most successful op amp ever. Fairchild, TI, and National still sell updated versions of this ubiquitous device. Fullagar, educated at Cambridge, U.K., and formerly employed at Ferranti, had joined Fairchild in 1966 following Widlar's departure after the µA702 and µA709 designs. Fullagar's µA741 creation incorporated internal compensation, short-circuit protection, and a novel high-impedance input stage to resolve shortcomings of the earlier designs. After leaving Fairchild, he joined Intersil as the company's first analog IC designer. The engineer-designer cofounded and became a vital technical contributor to Maxim Integrated Products in 1983; he retired in 1999.

The Output Stage The purpose of the output stage (Chapter 12 of the eighth edition) is to provide the amplifier with a low output resistance. In addition, the output stage should be able to supply relatively large load currents without dissipating an unduly large amount of power in the IC. The 741 uses an efficient class AB output stage, which we shall study in Section x5.1.3 of this supplement.

The output stage of the 741 consists of the complementary pair Q_{14} and Q_{20}, where Q_{20} is a *substrate pnp* (see Appendix A). Transistors Q_{18} and Q_{19} are fed by current source Q_{13A} and bias the output transistors Q_{14} and Q_{20}. Transistor Q_{23} (which is another substrate *pnp*) acts as an emitter follower, thus minimizing the loading effect of the output stage on the second stage.

Device Parameters In the following sections and exercises we carry out a detailed analysis of the 741 circuit. For the standard *npn* and *pnp* transistors, the following parameters will be used:

$$npn: \quad I_S = 10^{-14}\text{ A}, \beta = 200, V_A = 125\text{ V}$$

$$pnp: \quad I_S = 10^{-14}\text{ A}, \beta = 50, V_A = 50\text{ V}$$

In the 741 circuit the nonstandard devices are Q_{13}, Q_{14}, and Q_{20}. Transistor Q_{13} will be assumed to be equivalent to two transistors, Q_{13A} and Q_{13B}, with parallel base–emitter junctions and having the following saturation currents:

$$I_{SA} = 0.25 \times 10^{-14}\text{ A}$$

$$I_{SB} = 0.75 \times 10^{-14}\text{ A}$$

Transistors Q_{14} and Q_{20} will be assumed to each have an area three times that of a standard device. Output transistors usually have relatively large areas, to be able to supply large load currents and dissipate relatively large amounts of power with only a moderate increase in device temperature.

EXERCISE

x5.1 For the standard *npn* transistor whose parameters are given in Section x5.1 of this supplement, find approximate values for the following parameters at I_C = 0.1 mA: V_{BE}, g_m, r_e, r_π, and r_o.

Ans. 575 mV; 4 mA/V; 250 Ω; 50 kΩ; 1.25 MΩ

x5.1.2 DC Analysis

In this section, we shall carry out a dc analysis of the 741 circuit to determine the bias point of each device. For the dc analysis of an op-amp circuit, the input terminals are grounded. Theoretically speaking, this should result in zero dc voltage at the output. However, because the op amp has very large gain, any slight approximation in the analysis will show that the output voltage is far from being zero and is close to either $+V_{CC}$ or $-V_{EE}$. In actual practice, an op amp left open-loop will have an output voltage saturated close to one of the two supplies. To overcome this problem in the dc analysis, it will be assumed that the op amp is connected in a negative feedback loop that stabilizes the output dc voltage to zero volts.

Reference Bias Current The reference bias current I_{REF} is generated in the branch composed of the two diode-connected transistors Q_{11} and Q_{12} and resistor R_5. Thus,

$$I_{\text{REF}} = \frac{V_{CC} - V_{EB12} - V_{BE11} - (-V_{EE})}{R_5}$$

For $V_{CC} = V_{EE}$ = 15 V and $V_{BE11} = V_{EB12} \simeq 0.7$ V, we have I_{REF} = 0.73 mA.

Input-Stage Bias Transistors Q_{11} and Q_{10} and resistor R_4 form a Widlar current source (Section 8.7.4), thus

$$V_T \ln \frac{I_{\text{REF}}}{I_{C10}} = I_{C10} R_4 \qquad \text{(x5.1)}$$

EXERCISE

x5.2 Use Eq. (x5.1) to determine the value of I_{C10} by trial and error. Note that $I_{\text{REF}} = 0.73$ mA and $R_4 = 5$ kΩ.

Ans. $I_{C10} =$ 19 μA

Having determined I_{C10}, we proceed to determine the dc current in each of the input-stage transistors. For this purpose, we show in Fig. x5.2 the centerpiece of the input stage: As will be seen shortly, this is a negative-feedback circuit that stabilizes the bias current of each of Q_1 to Q_4 at a value approximately equal to $I_{C10}/2$. Refer to the analysis indicated in the diagram (where β_N is assumed to be high). The sum of the collector currents of Q_1 and Q_2 ($2I$) is fed to (or sensed by) the input of the current mirror Q_8–Q_9. The output current of the mirror, which for large β_P is approximately equal to $2I$, is compared to I_{C10} at node X. The difference between the two currents ($2I/\beta_P$) establishes the base currents of Q_3 and Q_4. This is the error signal of the feedback loop. For large β_P, this current approaches zero and a node equation at X gives $2I \simeq I_{C10}$, and thus $I \simeq I_{C10}/2$.

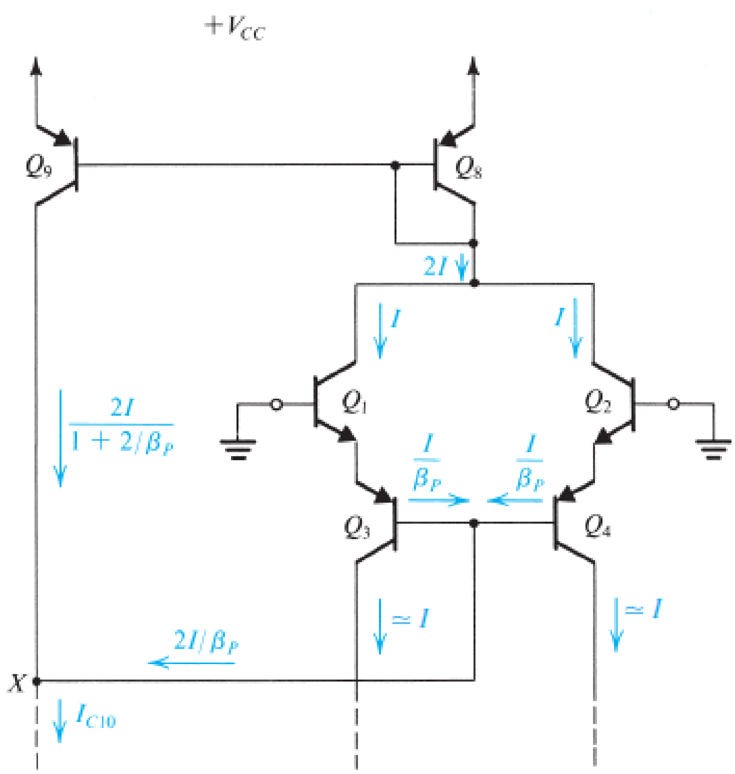

Figure x5.2 The dc analysis of the 741 input stage.

To verify the action of the negative-feedback loop in stabilizing the value of I, assume that for some reason I increases. We see that the input current of the Q_8–Q_9 mirror increases and, correspondingly, its output current increases. Assuming that I_{C10} remains constant, consideration of node X reveals that the base currents in Q_3 and Q_4 must decrease. This in turn decreases the value of I, which is opposite to the originally assumed change.

EXERCISES

x5.3 Using the value of I_{C10} found in Exercise x5.2, find the value of the bias current of each of Q_1, Q_2, Q_3, and Q_4.

Ans. 9.5 μA

x5.4 Determine the loop gain of the feedback loop in Fig. x5.2. Break the loop at the input of the Q_8–Q_9 mirror. Since the input resistance of the mirror is low, ground the connection of the collectors of Q_1 and Q_2. Apply an input test current i_t to the current mirror and find the feedback current that appears in the combined connection of the collectors of Q_1 and Q_2. Assume I_{C10} remains constant.

Ans. Loop gain $\simeq \beta_P$

Continuing with the dc analysis of the input stage, we show in Fig. x5.3 the current-mirror load (Q_5, Q_6, and Q_7) and the input transistor of the second stage (Q_{16}). The current-mirror load is fed by $I_{C3} = I_{C4} \simeq$ I. The analysis is illustrated in the figure and shows that for large β_N, each of Q_5 and Q_6 is biased at a current approximately equal to I. The bias current of Q_7 is somewhat higher, as shown in Exercise x5.5.

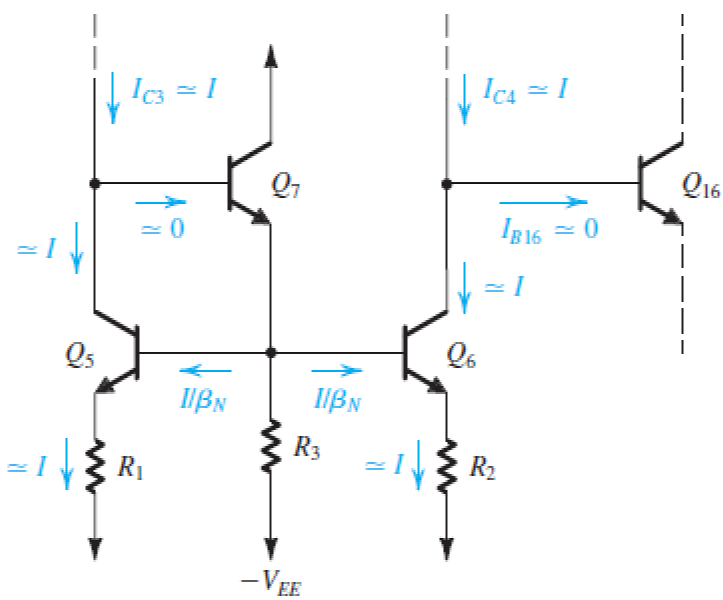

Figure x5.3 Continuation of the dc analysis of the 741 input stage.

EXERCISES

x5.5 Refer to Fig. x5.3 and recall that $I = 9.5\ \mu A$, $R_1 = R_2 = 1\ k\Omega$, $R_3 = 50\ k\Omega$, $\beta_N = 200$, and I_S (for all three transistors) is 10^{-14} A. Find V_{BE6}, V_{R3}, and I_{C7}.

Ans. 517 mV; 526.5 mV; 10.5 μA

x5.6 Recalling from Chapters 2 and 9 that the input bias current of an op amp is the average of its two input currents, thus

$$I_B = \frac{1}{2}(I_{B1} + I_{B2})$$

and the input offset current is

$$I_{OS} = |I_{B1} - I_{B2}|$$

find I_B and I_{OS} for the 741 if β_1 and β_2 are nominally 200 but can deviate from nominal by as much as ±5%.

Ans. 47.5 nA; 4.75 nA

Input Common-Mode Range The **input common-mode range** is the range of input common-mode voltages over which the input stage remains in the linear active mode. Refer to Fig. x5.1. We see that in the 741 circuit the input common-mode range is determined at the upper end by saturation of Q_1 and Q_2, and at the lower end by saturation of Q_3 and Q_4.

EXERCISE

x5.7 Neglect the voltage drops across R_1 and R_2 and assume that $V_{CC} = V_{EE} = 15$ V. Show that the input common-mode range of the 741 is approximately –12.9 V to +14.7 V. (Assume that $V_{BE} \simeq 0.6$ V and that to avoid saturation $V_{CB} \geq -0.3$ V for an *npn* transistor, and $V_{BC} \geq -0.3$ V for a *pnp* transistor.)

Second-Stage Bias If you refer to Fig. x5.1 you will see that if we neglect the base current of Q_{23}, the collector current of Q_{17} will be equal to the current supplied by Q_{13B}. We can then use I_{C17} to determine V_{BE17}, V_{B17}, the current through R_9 and hence I_{E16}, and finally $I_{C16} \simeq I_{E16}$.

EXERCISE

x5.8 Recalling that Q_{13B} has a scale current 0.75 times that of Q_{12}, find I_{C13B} and hence I_{C17}. Assume $\beta_P \gg 1$. Then determine V_{BE17}, I_{C16}, and I_{B16}. (Recall that $I_{REF} = 0.73$ mA, $I_S = 10{-}14$ A, and $\beta_N = 200$.)

Ans. 550 μA; 550 μA; 618 mV; 16.2 μA; 0.08 μA

Output Stage Bias Figure x5.4 shows the output stage of the 741 with the short-circuit protection circuitry omitted. Current source Q_{13A} delivers a current of $0.25I_{REF}$ (because I_S of Q_{13A} is 0.25 times the I_S of Q_{12}) to the network composed of Q_{18}, Q_{19}, and R_{10}. As mentioned in Section x5.1 of this supplement, the purpose of the Q_{18}–Q_{19} network is to establish two V_{BE} drops between the bases of the output transistors Q_{14} and Q_{20}. If we neglect the base currents of Q_{14} and Q_{20}, then the emitter current of Q_{23} will also be equal to $0.25I_{REF}$.

The determination of the bias currents of the output-stage transistors is illustrated by the following example.

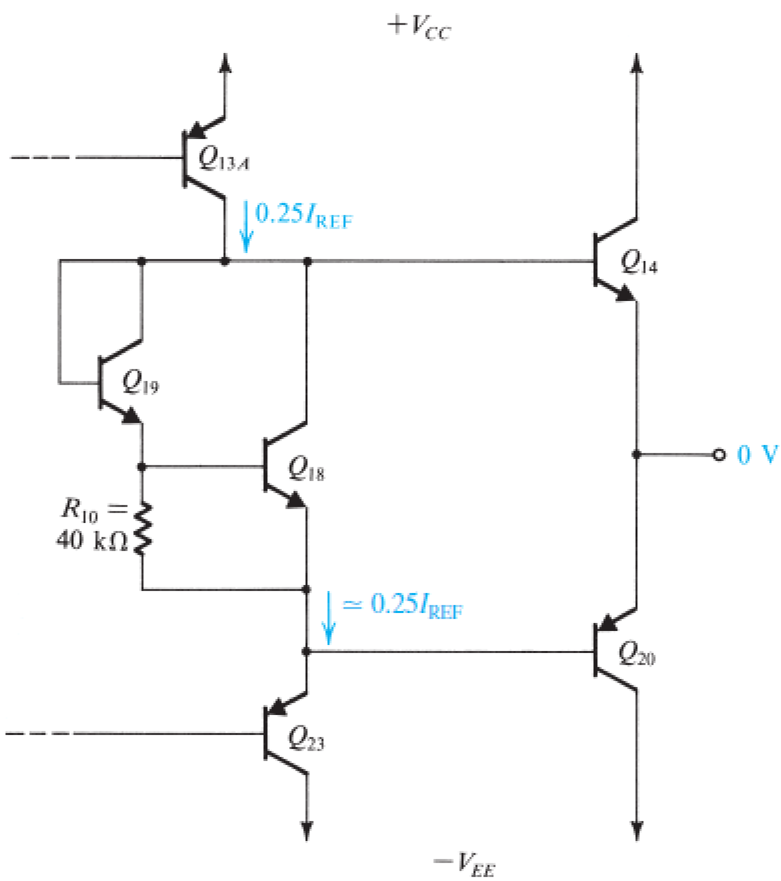

Figure x5.4 The 741 output stage without the short-circuit-protection devices.

Example x5.1

Determine I_{C23}, I_{B23}, $V_{BB} = V_{BE18} + V_{BE19}$, I_{C14}, and I_{C20}. Recall that Q_{14} and Q_{20} are nonstandard devices with $I_{S14} = I_{S20} = 3 \times 10^{-14}$ A.

Solution

Fig. x5.4 shows that

$$I_{C23} \simeq I_{E23} \simeq 0.25 I_{REF} = 180\ \mu\text{A}$$

Thus we see that the base current of Q_{23} is only 180/50 = 3.6 µA, which is negligible compared to I_{C17}, as we assumed before.

If we assume that V_{BE18} is approximately 0.6 V, we can determine the current in R_{10} as 15 µA. The emitter current of Q_{18} is therefore

$$I_{E18} = 180 - 15 = 165\mu\text{A}$$

Also,

$$I_{C18} \simeq I_{E18} = 165\mu\text{A}$$

At this value of current we find that V_{BE18} = 588 mV, which is quite close to the value assumed. The base current of Q_{18} is 165/200 = 0.8 µA, which can be added to the current in R_{10} to determine the Q_{19} current as

$$I_{C19} \simeq I_{E19} = 15.8\mu\text{A}$$

The voltage drop across the base–emitter junction of Q_{19} can now be determined as

$$V_{BE19} = V_T \ln \frac{I_{C19}}{I_S} = 530\ \text{mV}$$

The voltage drop V_{BB} can now be calculated as

$$V_{BB} = V_{BE18} + V_{BE19} = 588 + 530 = 1.118\ \text{V}$$

Since V_{BB} appears across the series combination of the base–emitter junctions of Q_{14} and Q_{20}, we can write

$$V_{BB} = V_T \ln \frac{I_{C14}}{I_{S14}} + V_T \ln \frac{I_{C20}}{I_{S20}}$$

Using the calculated value of V_{BB} and substituting $I_{S14} = I_{S20} = 3 \times 10^{-14}$ A, we determine the collector currents as

$$I_{C14} = I_{C20} = 154\ \mu\text{A}$$

This is the small current (relative to the load currents that the output stage is called upon to supply) at which the class AB output stage is biased.

Summary For future reference, Table x5.1 provides a listing of the values of the collector bias currents of the 741 transistors.

Table x5.1 DC Collector Currents of the 741 Circuit (μA)

Q_1	9.5	Q_8	19	Q_{13B}	550	Q_{19}	15.8
Q_2	9.5	Q_9	19	Q_{14}	154	Q_{20}	154
Q_3	9.5	Q_{10}	19	Q_{15}	0	Q_{21}	0
Q_4	9.5	Q_{11}	730	Q_{16}	16.2	Q_{22}	0
Q_5	9.5	Q_{12}	730	Q_{17}	550	Q_{23}	180
Q_6	9.5	Q_{13A}	180	Q_{18}	165	Q_{24}	
Q_7	10.5						

EXERCISE

x5.9 If in the circuit of Fig. x5.4 the Q_{18}–Q_{19} network is replaced by two diode-connected transistors, find the current in Q_{14} and Q_{20}. Assume that the diode-connected transistors utilize standard devices with $I_S = 10^{-14}$ A, while the nonstandard Q_{14} and Q_{20} have $I_S = 3 \times 10^{-14}$ A.

Ans. 540 μA

x5.1.3 Small-Signal Analysis

The Input Stage Figure x5.5 shows part of the 741 input stage for the purpose of performing small-signal analysis. Since the collectors of Q_1 and Q_2 are connected to a constant dc voltage, they are shown grounded. Also, the constant-current biasing of the bases of Q_3 and Q_4 is equivalent to having the common-base terminal open-circuited.

The differential signal v_i applied between the input terminals effectively appears across four equal emitter resistances connected in series—those of Q_1, Q_2, Q_3, and Q_4. As a result, emitter signal currents flow as indicated in Fig. x5.5 with

$$i_e = \frac{v_i}{4r_e} \qquad \text{(x5.2)}$$

where r_e denotes the emitter resistance of each of Q_1 through Q_4. Thus

$$r_e = \frac{V_T}{I}$$

Thus the four transistors Q_1 through Q_4 supply the load circuit with a pair of complementary current signals αi_e, as indicated in Fig. x5.5.

The input differential resistance of the op amp can be obtained from Fig. x5.5 as

$$R_{id} = 4(\beta_N + 1)r_e \qquad \text{(x5.3)}$$

Proceeding with the input-stage analysis, we show in Fig. x5.6 the current-mirror-load circuit fed with the complementary pair of current signals found earlier. The analysis, together with the order of the steps in which it is performed, is indicated on the diagram. As expected, the current mirror provides an output current i_o,

$$i_o = 2\alpha i_e \tag{x5.4}$$

Combining Eqs. (x5.2) and (x5.4) provides the transconductance of the input stage as

$$G_{m1} \equiv \frac{i_o}{v_i} = \frac{\alpha}{2r_e} = \frac{1}{2}g_{m1} \tag{x5.5}$$

where g_{m1} is the transconductance of each of the four transistors Q_1, Q_2, Q_3, and Q_4.

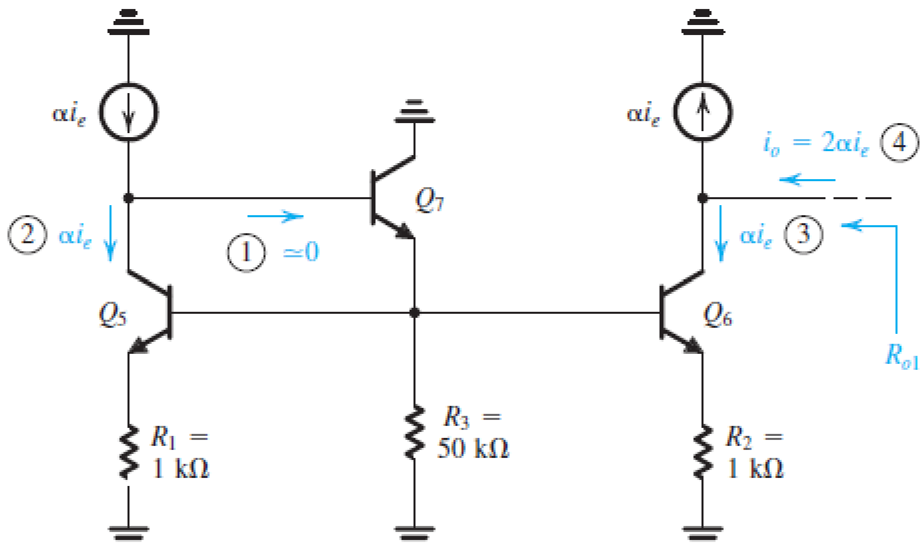

Figure x5.6 The current-mirror-load circuit of the input stage fed by the two complementary current signals generated by Q_1 through Q_4 in Fig. x5.5. Circled numbers indicate the order of the analysis steps.

EXERCISES

x5.10 Recalling that each of the input-stage transistors is biased at a current I = 9.5 µA and that β_N = 200, find r_e, g_{m1}, G_{m1}, and R_{id}.

Ans. 2.63 kΩ; 0.38 mA/V; 0.19 mA/V; 2.1MΩ

x5.11 For the circuit in Fig. x5.6, find the following in terms of i_e: (a) the signal voltage at the base of Q_6; (b) the signal current in the emitter of Q_7; (c) the signal current in the base of Q_7; (d) the signal voltage at the base of Q_7; (e) the input resistance seen by the left-hand-side signal current source αi_e. Assume that $I_{C7} \simeq I_{C5} = I_{C6}$, and use the results of Exercise x5.10.

Ans. (a) 3.63 kΩ × i_e; (b) $0.08 i_e$; (c) $0.0004 i_e$; (d) 3.84 kΩ × i_e; (e) 3.84 kΩ

To complete our modeling of the 741 input stage, we must find its output resistance R_{o1}. This is the resistance seen "looking back" into the output terminal of the circuit in Fig. x5.6. Thus R_{o1} is the parallel equivalent of the output resistance of the current source supplying the signal current αi_e, and the output resistance of Q_6. The first component is the resistance looking into the collector of Q_4 in Fig. x5.5. Finding this resistance is considerably simplified if we assume that the common bases of Q_3 and Q_4 are at a *virtual ground*. This of course happens only when the input signal v_i is applied in a complementary fashion. Nevertheless, making this assumption does not result in a large error.

Assuming that the base of Q_4 is at virtual ground, the resistance we are after is R_{o4}, shown in Fig. x5.7(a). This is the output resistance of a common-base transistor that has a resistance (r_e of Q_2) in its emitter. To find R_{o4} we use the following expression (Eq. 8.70):

$$R_o = r_o[1 + g_m(R_e \| r_\pi)] \quad \text{(x5.6)}$$

where $R_e = r_e$ and $r_o = V_{Ap}/I$.

The second component of the output resistance is that seen looking into the collector of Q_6 in Fig. x5.6 with the αi_e generator set to 0. Although the base of Q_6 is not at signal ground, we shall assume that the signal voltage at the base is small enough to make this approximation valid. The circuit then takes the form shown in Fig. x5.7(b), and R_{o6} can be determined using Eq. (x5.6) with $R_e = R_2$.

Figure x5.8 shows the equivalent circuit that we have derived for the input stage.

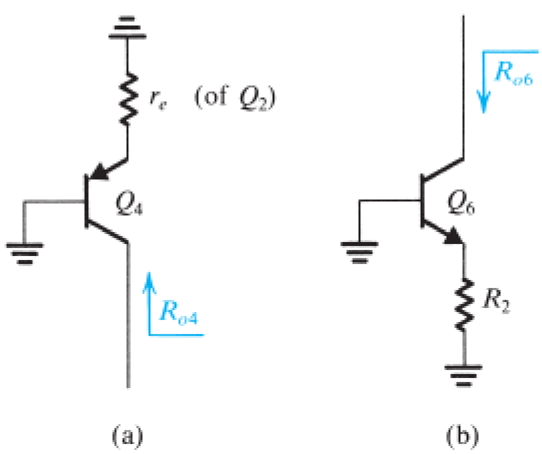

Figure x5.7 Simplified circuits for finding the two components of the output resistance R_{o1} of the first stage.

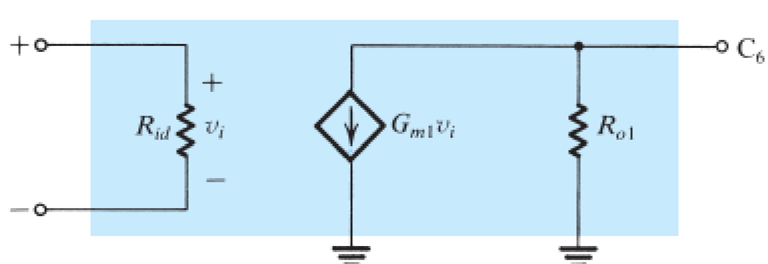

Figure x5.8 Small-signal equivalent circuit for the input stage of the 741 op amp.

EXERCISES

x5.12 Find the values of R_{o4} and R_{o6} and thus the output resistance of the first stage, R_{o1}. Recall that $I = 9.5\ \mu A$, $V_{an} = 125$ V, $V_{Ap} = 50$ V, $R_2 = 1$ kΩ, $\beta_N = 200$, and $\beta_P = 50$.

Ans. 10.5 MΩ; 18.2 MΩ; 6.7 MΩ

x5.13 Use the equivalent circuit of Fig. x5.8 together with the value of G_{m1} found in Exercise x5.10 and the value of R_{o1} found in Exercise x5.12 to determine the open-circuit voltage gain of the 741 input stage.

Ans. $|A_{vo}| = G_{m1}R_{o1} = 1273$ V/V

Example x5.2

We wish to find the input offset voltage resulting from a 2% mismatch between the resistances R_1 and R_2 in Fig. x5.1.

Solution

Consider first the situation when both input terminals are grounded, and assume that $R_1 = R$ and $R_2 = R + \Delta R$, where $\Delta R/R = 0.02$. From Fig. x5.9 we see that while Q5 still conducts a current equal to I, the current in Q6 will be smaller by ΔI. The value of ΔI can be found from

$$V_{BE5} + I_R = V_{BE6} + (I - \Delta I)(R + \Delta R)$$

Thus,

$$V_{BE5} - V_{BE6} = I\Delta R - \Delta I\,(R + \Delta R) \tag{x5.7}$$

The quantity on the left-hand side is in effect the change in V_{BE} due to a change in I_E of ΔI. We may therefore write

$$V_{BE5} - V_{BE6} \simeq \Delta I r_e \tag{x5.8}$$

Equations (x5.7) and (x5.8) can be combined to obtain

$$\frac{\Delta I}{I} = \frac{\Delta R}{R + \Delta R + r_e} \tag{x5.9}$$

Substituting $R = 1$ kΩ and $r_e = 2.63$ kΩ shows that a 2% mismatch between R_1 and R_2 gives rise to an output current $\Delta I = 5.5 \times 10^{-3} I$. To reduce this output current to zero we have to apply an input voltage V_{OS} given by

$$V_{OS} = \frac{\Delta I}{G_{m1}} = \frac{5.5 \times 10^{-3} I}{G_{m1}} \quad \text{(x5.10)}$$

Substituting $I = 9.5$ μA and $G_{m1} = 0.19$ mA/V results in the offset voltage $V_{OS} \simeq 0.3$ mV.

It should be pointed out that the offset voltage calculated is only one component of the input offset voltage of the 741. Other components arise because of mismatches in transistor characteristics. The 741 offset voltage is specified to be typically 2 mV.

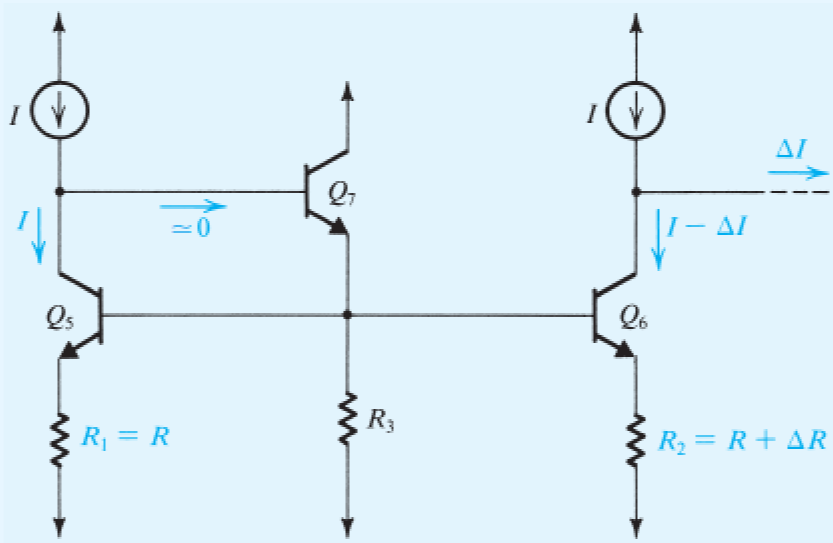

Figure x5.9 Input stage with both inputs grounded and a mismatch ΔR between R_1 and R_2.

Example x5.3

We are required to find the CMRR of the 741 input stage. Assume that the circuit is balanced except for mismatches in the current-mirror load that result in an error ϵ_m in the mirror's current-transfer ratio; that is, the ratio becomes $(1 - \epsilon_m)$.

Solution

In Section 9.5.5 we analyzed the common-mode operation of the current-mirror-loaded differential amplifier and derived an expression for its CMRR. The situation in the 741 input stage, however, differs substantially because of the feedback loop that regulates the bias current. Since this feedback loop is sensitive to the common-mode signal, as will be seen shortly, the loop operates to reduce the common-mode gain and, correspondingly, to increase the CMRR. Hence, its action is referred to as **common-mode feedback**.

Figure x5.10 shows the 741 input stage with a common-mode signal v_{icm} applied to both input terminals. We have assumed that as a result of v_{icm}, a signal current i flows as shown. Since the stage is balanced, both sides carry the same current i.

Our objective now is to determine how i relates to v_{icm}. Toward that end, observe that for common-mode inputs, both sides of the differential amplifier, that is, Q_1–Q_3 and Q_2–Q_4, act as followers, delivering a signal almost equal to v_{icm} to the common-base node of Q_3 and Q_4. Now, this node Y is connected to the collectors of two current sources, Q_9 and Q_{10}. Denoting the total resistance between node Y and ground R_o, we write

$$R_o = R_{o9} \parallel R_{o10} \tag{x5.11}$$

In Fig. x5.10 we have "pulled R_o out," thus leaving behind ideal current sources Q_9 and Q_{10}. Since the current in Q_{10} is constant, we show Q_{10} in Fig. x5.10 as having a zero incremental current. Transistor Q_9, on the other hand, provides a current approximately equal to that fed into Q_8, which is $2i$. This is the feedback current. Since Q_8 senses the *sum* of the currents in the two sides of the differential amplifier, the feedback loop operates only on the common-mode signal and is insensitive to any difference signal.

Proceeding with the analysis, we now can write a node equation at Y,

$$2i + \frac{2i}{\beta_P} = \frac{v_{icm}}{R_o} \tag{x5.12}$$

Assuming $\beta_P \gg 1$, this equation simplifies to

$$i \simeq \frac{v_{icm}}{sR_o} \tag{x5.13}$$

Having determined i, we now proceed to complete our analysis by finding the output current i_o. From the circuit in Fig. x5.10, we see that

$$i_o = \epsilon_m i \tag{x5.14}$$

Thus the common-mode transconductance of the input stage is given by

$$G_{mcm} \equiv \frac{i_o}{v_{icm}} = \frac{\epsilon_m i}{v_{icm}}$$

Substituting for i from Eq. (x5.13) gives

$$G_{mcm} = \frac{\epsilon_m}{2R_o} \tag{x5.15}$$

Finally, the CMRR can be found as the ratio of the differential transconductance G_{m1} found in Eq. (x5.5) and the common-mode transconductance G_{mcm},

$$\text{CMRR} \equiv \frac{G_{m1}}{G_{mcm}} = g_{m1} R_o / \epsilon_m \tag{x5.16}$$

where g_{m1} is the transconductance of Q_1. Now substituting for R_o from Eq. (x5.11), we obtain

$$\text{CMRR} = g_{m1}\,(R_{o9} \| R_{o10}) / \epsilon_m \tag{x5.17}$$

Before leaving this example, we observe that if the feedback were not present, the 2i term in Eq. (x5.12) would be absent and the current i would become $\beta_P\,(v_{icm}/2R_o)$, which is β_P times higher than that when feedback is present. In other words, common-mode feedback reduces i, hence the common-mode transconductance and the common-mode gain, by a factor β_P. It can be shown that β_P is the magnitude of the loop gain. (See Exercise x5.4.)

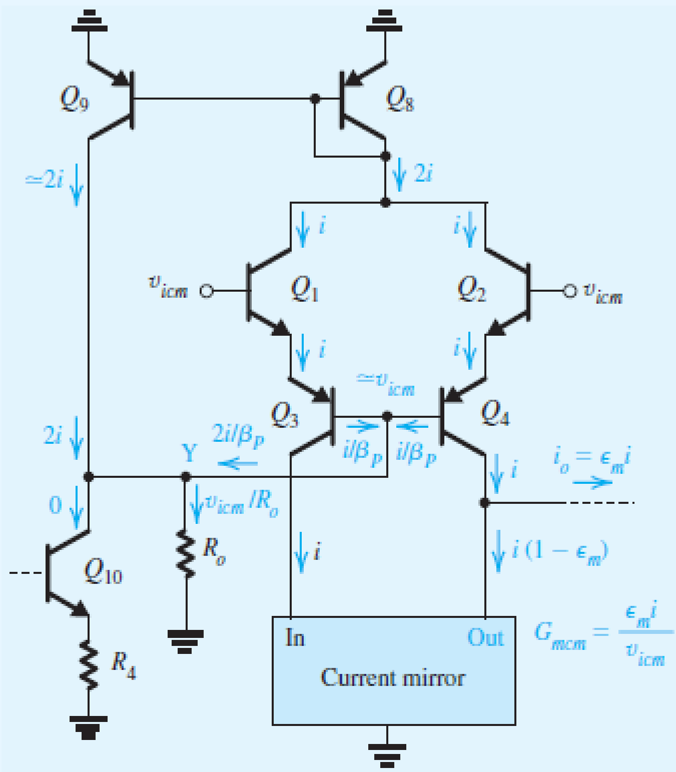

Figure x5.10 Example x5.3: Analysis of the common-mode gain of the 741 input stage. Note that $R_o = R_{o9} \parallel R_{o10}$ has been "pulled out" and shown separately, leaving behind ideal current sources Q_9 and Q_{10}.

EXERCISES

x5.14 Show that if the source of the imbalance in the current-mirror load is that while $R_1 = R$, $R_2 = R + \Delta R$, the error ϵ_m is given by

$$\epsilon_m = \frac{\Delta R}{R + r_{es} + \Delta R}$$

Evaluate ϵ_m for $\Delta R/R = 0.02$.

Ans. $\epsilon_m = 5.5 \times 10^{-3}$

x5.15 Refer to Fig. x5.10 and assume that the bases of Q_9 and Q_{10} are at approximately constant voltages (signal ground). Find R_{o9}, R_{o10}, and hence R_o. Use V_A = 125 V for *npn* and 50 V for *pnp* transistors. Use the bias current values in Table 13.1.

Ans. R_{o9} = 2.63 MΩ; R_{o10} = 31.1 MΩ; R_o = 2.43 MΩ

x5.16 Use the results of Exercises x5.14 and x5.15 to determine G_{mcm} and CMRR of the 741 input stage. What would the CMRR be if the common-mode feedback were not present? Assume $\beta_P = 50$.

Ans. $G_{mcm} = 1.13 \times 10^{-6}$ mA/V; CMRR = 1.68×10^5 or 104.5 dB; without common-mode feedback, CMRR = 70.5 dB

The Second Stage Figure x5.11(a) shows the 741 second stage prepared for small-signal analysis, and Fig. x5.11(b) shows its small-signal model. The three model parameters R_{i2}, G_{m2}, and R_{o2} can be determined as follows.

The input resistance R_{i2} can be found by inspection to be

$$R_{i2} = (\beta_{16} + 1)\{r_{e16} + [R_9 \,||\, (\beta_{17} + 1)(r_{e17} + R_8)]\} \qquad \text{(x5.18)}$$

From the equivalent circuit of Fig. x5.11(b), we see that the transconductance G_{m2} is the ratio of the *short-circuit output current* to the input voltage. Short-circuiting the output terminal of the second stage (Fig. x5.11a) to ground makes the signal current through the output resistance of Q_{13B} zero, and the output short-circuit current becomes equal to the collector signal current of Q_{17} (i_{c17}). This latter current can be easily related to v_{i2} as follows:

$$i_{c17} = \frac{\alpha v_{b17}}{r_{e17} + R_8} \qquad \text{(x5.19)}$$

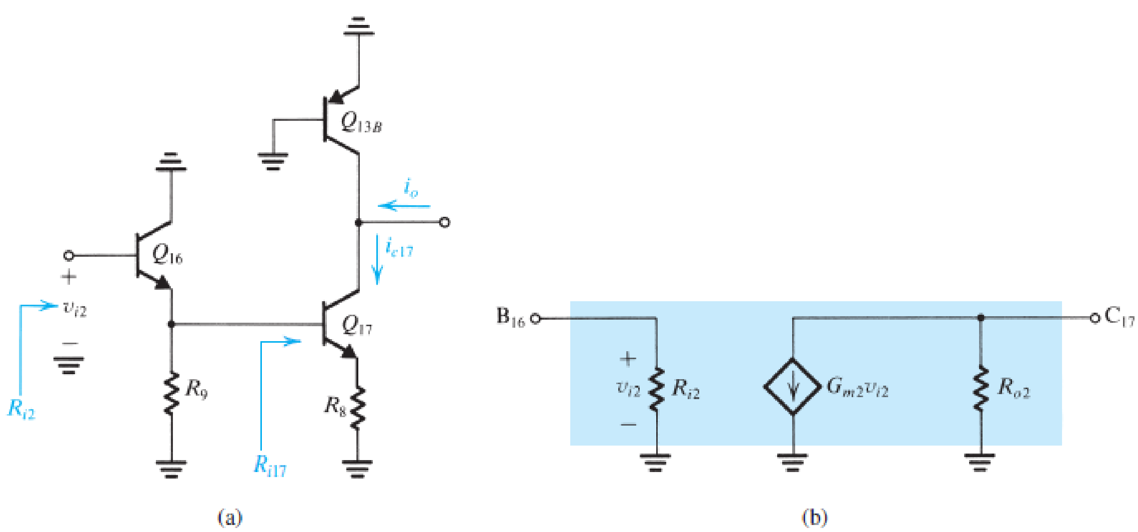

Figure x5.11 **(a)** The 741 second stage prepared for small-signal analysis. **(b)** Equivalent circuit.

$$v_{b17} = v_{i2}\frac{(R_9 \| R_{i17})}{(R_9 \| R_{i17}) + r_{e16}} \tag{x5.20}$$

$$R_{i17} = (\beta_{17} + 1)(r_{e17} + R_8) \tag{x5.21}$$

where we have neglected r_{o16} because $r_{o16} \gg R_9$. These equations can be combined to obtain

$$G_{m2} \equiv \frac{i_{c17}}{v_{i2}} \tag{x5.22}$$

To determine the output resistance R_{o2} of the second stage in Fig. x5.11(a), we ground the input terminal and find the resistance looking back into the output terminal. It follows that R_{o2} is given by

$$R_{o2} = (R_{o13B} \| R_{o17}) \tag{x5.23}$$

where R_{o13B} is the resistance looking into the collector of Q_{13B} while its base and emitter are connected to ground. It can be easily seen that

$$R_{o13B} = r_{o13B} \tag{x5.24}$$

The second component in Eq. (x5.23), R_{o17}, is the resistance seen looking into the collector of Q_{17}. Since the resistance between the base of Q_{17} and ground is relatively small (approximately equal to r_{e16}), one can considerably simplify matters by assuming that the base is grounded. Doing this, we can use Eq. (x5.6) to determine R_{o17}.

EXERCISES

In the following exercises use I_{C13B} = 550 μA, I_{C16} = 16.2 μA, I_{C17} = 550 μA, β_N = 200, β_P = 50, V_{An} = 125 V, V_{Ap} = 50 V, R_9 = 50 kΩ, and R_8 = 100 Ω.

x5.17 Determine the value of R_{i2}.

Ans. 4 MΩ

x5.18 Determine the value of G_{m2}.

Ans. 6.5 mA/V

x5.19 Determine the values of R_{o13B}, R_{o17}, and R_{o2}.

Ans. 90.9 kΩ; 722 kΩ; 81 kΩ

x5.20 Determine the value of the open-circuit voltage gain of the second stage.

Ans. −526.5 V/V

The Output Stage The 741 output stage is shown in Fig. x5.12 without the short-circuit protection circuitry. The stage is shown driven by the second-stage transistor Q_{17} and loaded with a 2-kΩ resistance. The circuit is of the AB class (Section 12.4), with the network composed of Q_{18}, Q_{19}, and R_{10} providing the bias of the output transistors Q_{14} and Q_{20}. The use of this network rather than two diode-connected transistors in series enables biasing the output transistors at a low current (0.15 mA) in spite of the fact that the output devices are three times as large as the standard devices. This result is obtained by arranging that the current in Q_{19} is very small and thus its V_{BE} is also small. We analyzed the dc bias in Section x5.2 of the bonus material.

Another feature of the 741 output stage worth noting is that the stage is driven by an emitter follower Q_{23}. As will be shown, this emitter follower provides added buffering, which makes the op-amp gain almost independent of the parameters of the output transistors.

Let's first determine the allowable range of output voltage swing. The maximum positive output voltage is limited by the saturation of current-source transistor Q_{13A}. Thus,

$$v_{O\max} = V_{CC} - |V_{CEsat}| - V_{BE14} \tag{x5.25}$$

which is about 1 V below V_{CC}. The minimum output voltage (i.e., maximum negative amplitude) is limited by the saturation of Q_{17}.

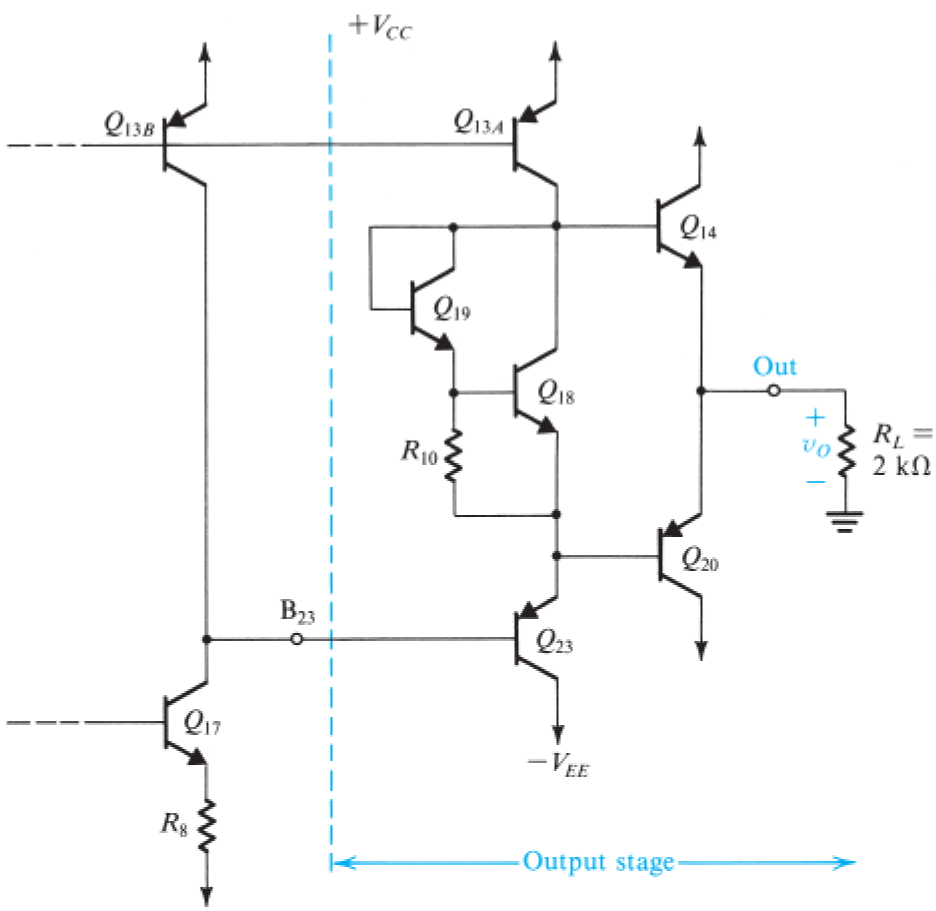

Figure x5.12 The 741 output stage without the short-circuit-protection circuitry.

Neglecting the voltage drop across R_8, we obtain

$$v_{O\min} = -V_{EE} + V_{CEsat} + V_{EB23} + V_{EB20} \quad \text{(x5.26)}$$

which is about 1.5 V above $-V_{EE}$.

Next, we consider the small-signal analysis of the output stage. Specifically, we model the output stage using the equivalent circuit in Fig. x5.13 and determine the model parameters as follows. Note that the model is shown fed with the open-circuit voltage of the second stage v_{o2}, where from Fig. x5.11(b), $v_{o2} = -G_{m2}R_{o2}v_{i2}$.

To determine the input resistance R_{in3}, we take into account the load resistance R_L and assume that one of the output transistors is conducting, as shown in the following example.

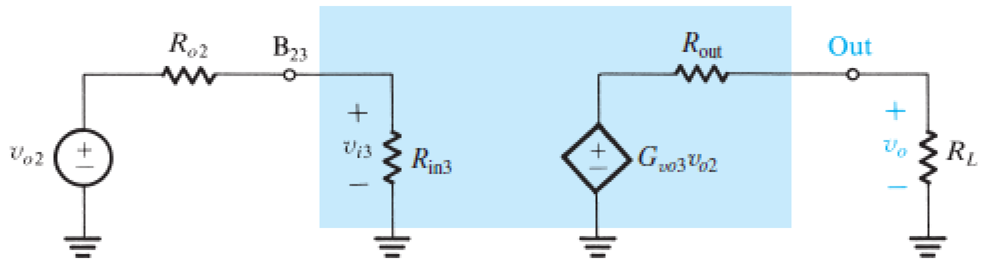

Figure x5.13 Model for the 741 output stage in Fig. x5.12.

Example x5.4

Assuming that Q_{14} is off and Q_{20} is conducting a current of 5 mA to a load R_L = 2 kΩ, determine the value of R_{in3}. Using G_{m2} = 6.5 mA/V and R_{o2} = 81 kΩ, determine the voltage gain of the second stage.

Solution

Refer to Fig. x5.12. The input resistance looking into the base of Q_{20} is approximately $\beta_{20}R_L$ = 50 ×2 = 100 kΩ. This resistance appears in parallel with the series combination of $r_{o13A} = V_{Ap}/I_{C13A}$ = 50V/180 μA = 280 kΩ, and the resistance of the Q_{18}–Q_{19} network. The latter resistance is very small (about 160 Ω; see later: Exercise x5.22). Thus, the total resistance in the emitter of Q_{23} is approximately (100 kΩ ∥ 280 kΩ) or 74 kΩ, and the input resistance R_{in3} is obtained as

$$R_{in3} = \beta_{23} \times 74 \text{ k}\Omega = 50 \times 74 = 3.7 \text{ M}\Omega$$

We thus see that $R_{in3} \gg R_{o2}$, and the value of R_{in3} will have little effect on the performance of the op amp. Still we can determine the gain of the second stage as

$$A_2 \equiv \frac{v_{i3}}{v_{i2}} = -G_{m2}R_{o2}\frac{R_{in3}}{R_{in3}+R_{o2}}$$

$$= -6.5 \times 81 \frac{3700}{3700+81} = -515 \text{ V/V}$$

Continuing with the determination of the equivalent-circuit model parameters, we note from Fig. x5.13 that G_{vo3} is the **open-circuit overall voltage gain** of the output stage,

$$G_{vo3} = \left.\frac{v_o}{v_{o2}}\right|_{R_L=\infty} \qquad \text{(x5.27)}$$

With $R_L = \infty$, the gain of the emitter-follower output transistor (Q_{14} or Q_{20}) will be nearly unity. Also, with $R_L = \infty$ the resistance in the emitter of Q_{23} will be very large. This means that the gain of Q_{23} will be nearly unity and the input resistance of Q_{23} will be very large. We thus conclude that $G_{vo3} \simeq 1$.

Next, we shall find the value of the output resistance of the op amp, R_{out}. For this purpose, refer to the circuit shown in Fig. x5.14. In accordance with the definition of R_{out} from Fig. x5.13, the input source feeding the output stage is grounded, but its resistance (which is the output resistance of the second stage, R_{o2}) is included. We have assumed that the output voltage v_O is negative, and thus Q_{20} is conducting most of the current; transistor Q_{14} has therefore been eliminated. The exact value of the output resistance will of course depend on which transistor (Q_{14} or Q_{20}) is conducting and on the value of load current. Nevertheless, we wish to find an estimate of R_{out} . The analysis for doing so is shown in Fig. x5.14. It should be noted, however, that to the value of R_{out} given in the figure we must add the resistance R_7 (27 Ω) (see Fig. x5.1), which is included for short-circuit protection, in order to obtain the total output resistance of the 741.

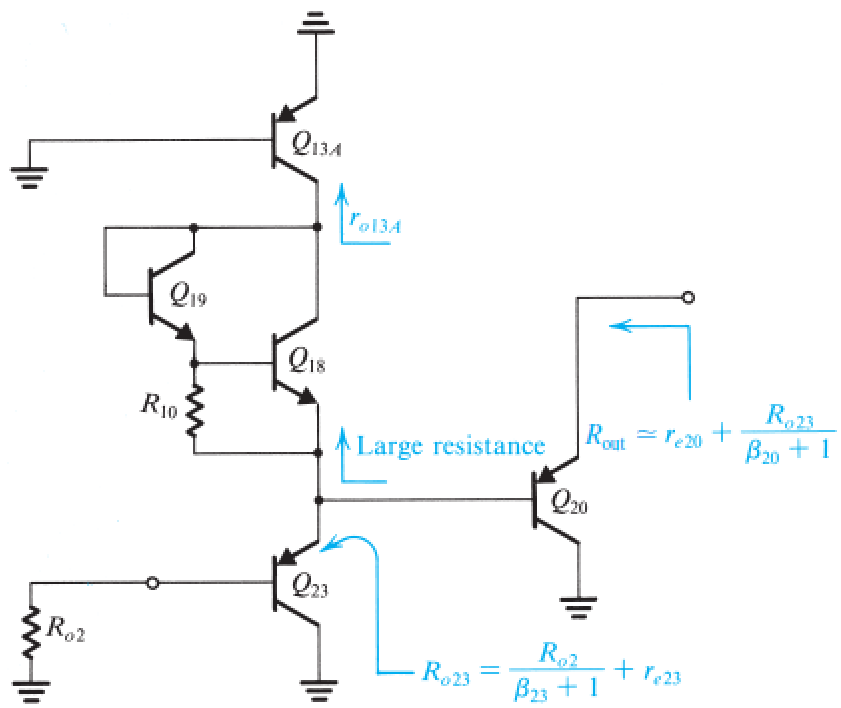

Figure x5.14 Circuit for finding the output resistance R_{out} .

EXERCISES

x5.21 Find the value of R_{o23}, R_{out}, and the total output resistance of the 741 op amp. Use R_{o2} = 81 kΩ, $\beta_{23} = \beta_{20}$ = 50, and I_{C23} = 180 µA, and assume that Q_{20} is conducting a load current of 5 mA.

Ans. 1.73 k Ω; 39 Ω; 66 Ω

x5.22 Using a simple (r_π , g_m) model for each of the two transistors Q_{18} and Q_{19} in Fig. x5.15, find the small-signal resistance between *A* and *A′*. (Note: From Table x5.1, I_{C18} = 165 µA and I_{C19} ≃ 16 µA. Also, β_N = 200.)

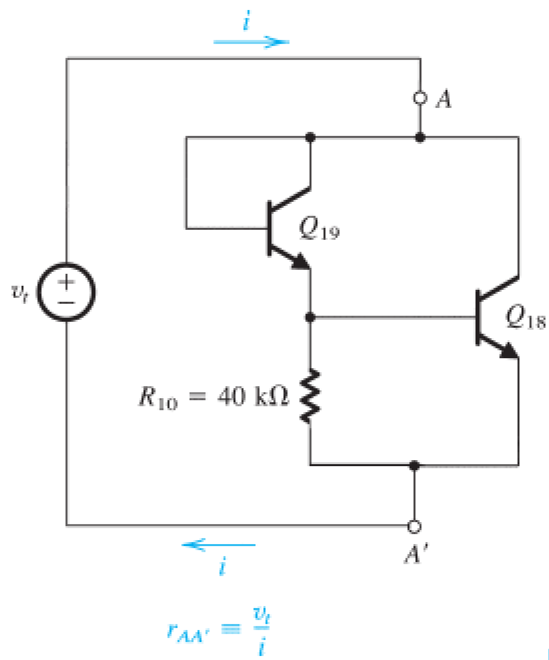

Figure x5.15

Ans. 163 Ω

Output Short-Circuit Protection If the op-amp output terminal is short-circuited to one of the power supplies, one of the two output transistors could conduct a large amount of current. Such a large current can result in sufficient heating to cause burnout of the IC (Chapter 12). To guard against this possibility, the 741 op amp is equipped with a special circuit for short-circuit protection. The function of this circuit is to limit the current in the output transistors in the event of a short circuit.

Refer to Fig. x5.1 and note that the short-circuit-protection circuitry is highlighted in color. Resistance R_6 together with transistor Q_{15} limits the current that would flow out of Q_{14} in the event of a short circuit. Specifically, if the current in the emitter of Q_{14} exceeds about 20 mA, the voltage drop across R_6 exceeds 540 mV, which turns Q_{15} on. As Q_{15} turns on, its collector robs some of the current supplied by Q_{13A}, thus reducing the base current of Q_{14}. This mechanism thus limits the maximum current that the op amp can source (i.e., supply from the output terminal in the outward direction) to about 20 mA.

Limiting of the maximum current that the op amp can sink, and hence the current through Q_{20}, is done by a mechanism similar to the one discussed above. The relevant circuit is composed of R_7, Q_{21}, Q_{24}, and Q_{22}. For the components shown, the current in the inward direction is limited also to about 20 mA.

Overall Voltage Gain The overall small-signal gain can be found from the cascade of the equivalent circuits derived above for the three op-amp stages. This cascade is shown in Fig. x5.16, loaded with R_L = 2 kΩ, which is the typical value used in measuring and specifying the 741 data. The overall gain can be expressed as

$$\frac{v_o}{v_i} = \frac{v_{i2}}{v_i}\frac{v_{o2}}{v_{i2}}\frac{v_o}{v_{o2}}$$

$$= -G_{m1}(R_{o1}\|R_{i2})(-G_{m2}R_{o2})G_{vo3}\frac{R_L}{R_L + R_{\text{out}}} \quad \text{(x5.28)}$$

Using the values found earlier yields for the overall open-circuit voltage gain,

$$A_0 \equiv \frac{v_o}{v_i} = -476.1 \times (-526.5) \times 0.97 = 243{,}147\,\frac{\text{V}}{\text{V}}$$

$$= 107.7\text{ dB} \quad \text{(x5.29)}$$

x5.1.4 Frequency Response

The 741 is an internally compensated op amp. It employs the Miller compensation technique, studied in Section 11.10.3, to introduce a dominant low-frequency pole. Specifically, a 30-pF capacitor (C_C) is connected in the negative-feedback path of the second stage. An approximate estimate of the frequency of the dominant pole can be obtained as follows.

From Miller's theorem (Section 10.2.5), we see that the effective capacitance due to C_C between the base of Q_{16} and ground is (see Fig. x5.1)

$$C_{\text{in}} = C_C(1 + |A_2|) \quad \text{(x5.30)}$$

where A_2 is the second-stage gain. Use of the value calculated for A_2 found in Example x5.4, $A_2 = -515$, results in C_{in} = 15,480 pF. Since this capacitance is quite large, we shall neglect all other capacitances between the base of Q_{16} and signal ground. The total resistance between this node and ground is

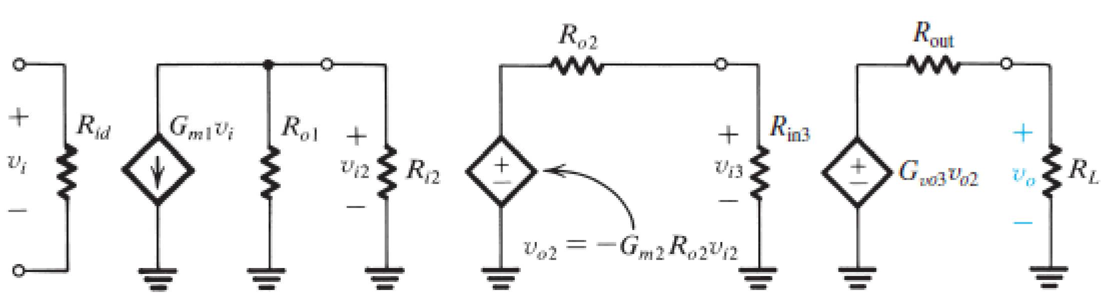

Figure x5.16 Cascading the small-signal equivalent circuits of the individual stages for the evaluation of the overall voltage gain.

$$R_t = R_{o1} \| R_{i2}$$
$$= 6.7\ \text{M}\Omega \| 4\ \text{M}\Omega = 2.5\ \text{M}\Omega \quad \text{(x5.31)}$$

Thus the dominant pole has a frequency f_P given by

$$f_P = \frac{1}{2\pi C_{\text{in}} R_t} = 4.1\ \text{Hz} \quad \text{(x5.32)}$$

Note that this approach is equivalent to using the appropriate formula in Eq. (11.58) found in the textbook.

As discussed in Section 11.10.3, Miller compensation provides an additional advantageous effect, namely, pole splitting. As a result, the other poles of the circuit are moved to very high frequencies. This has been confirmed by computer-aided analysis (see Gray et al., 2000).

Assuming that all nondominant poles are at very high frequencies, the calculated values give rise to the Bode plot shown in Fig. x5.17, where $f_{3\text{dB}} = f_P$. The unity-gain bandwidth f_t can be calculated from

$$f_t = A_0 f_{3\text{dB}} \quad \text{(x5.33)}$$

Thus,

$$f_t = 243{,}147 \times 4.1 \simeq 1\ \text{MHz} \quad \text{(x5.34)}$$

Although this Bode plot implies that the phase shift at f_t is –90° and thus that the phase margin is 90°, in practice a phase margin of about 80° is obtained. The excess phase shift (about 10°) is due to the nondominant poles. This phase margin is sufficient to provide stable operation of closed-loop amplifiers with any value of feedback factor β.

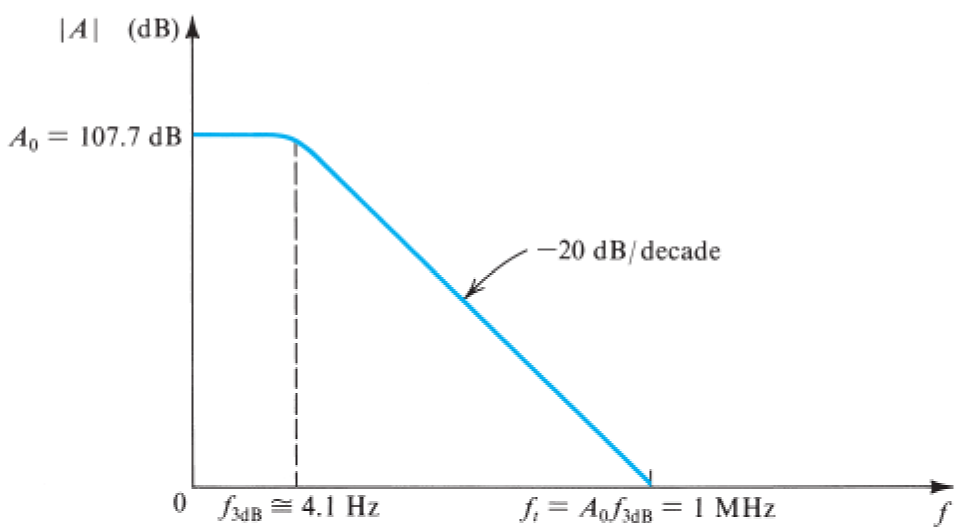

Figure x5.17 Bode plot for the 741 gain, neglecting nondominant poles.

This convenience of use of the internally compensated 741 is achieved at the expense of a great reduction in open-loop gain and hence in the amount of negative feedback. In other words, if one requires a closed-loop amplifier with a gain of 1000, then the 741 is *overcompensated* for such an application, and one would be much better off designing one's own compensation (assuming, of course, the availability of an op amp that is not already internally compensated).

A Simplified Model The simplified model of the 741 op amp shown in Fig. x5.18 is similar to what we used for the CMOS two-stage op amp (Section 13.1.5). Here, however, the high-gain second stage, with its feedback capacitance C_C, is modeled by an ideal integrator. In this model, the gain of the second stage is assumed to be sufficiently large that a virtual ground appears at its input. For this reason the output resistance of the input stage and the input resistance of the second stage have been omitted. Furthermore, the output stage is assumed to be an ideal unity-gain follower. (Of course, the two-stage CMOS amplifier does not have an output stage.)

Analysis of the model in Fig. x5.18 gives

$$A(s) \equiv \frac{V_o(s)}{V_i(s)} = \frac{G_{m1}}{sC_C} \tag{x5.35}$$

Thus,

$$A(j\omega) = \frac{G_{m1}}{j\omega C_C} \tag{x5.36}$$

Substituting Gm1 – 0.19 mA/V and CC = 30 pF yields

$$f_t = \frac{\omega_t}{2\pi} \simeq 1 \text{ MHz} \tag{x5.37}$$

which is equal to the value calculated before. It should be pointed out, however, that this model is valid only at frequencies $f \gg f_{3dB}$. At such frequencies, the gain falls off with a slope of –20 dB/decade (Fig. x5.17), just like that of an integrator.

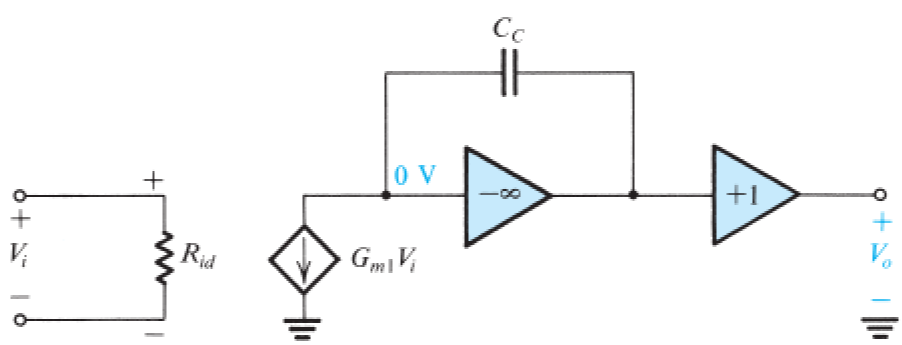

Figure x5.18 A simple model for the 741 based on modeling the second stage as an integrator.

x5.1.5 Slew Rate

The slew-rate limitation of op amps is discussed in Chapter 2, and expressions for *SR* are derived for the two-stage CMOS op amp in Section 13.1 and for the folded-cascode CMOS op amp in Section 13.2. The 741 slewing is very similar to that of the two-stage CMOS op amp. Thus, following an identical procedure, we can show that for the 741 op amp,

$$SR = \frac{2I}{C_C} \tag{x5.38}$$

where $2I$ is the total bias current of the input differential stage. For the 741, $I = 9.5\ \mu\text{A}$, and $C_C = 30$ pF, resulting in $SR = 0.63\ \text{V}/\mu\text{s}$.

Also, as we have done for the two-stage CMOS op amp, we can derive a relationship between *SR* and ω_t. For the 741 case, we can show that

$$SR = 4\,V_T\omega_t \tag{x5.39}$$

where V_T is the thermal voltage (approximately 25 mV at room temperature). As a check, for the 741 we have

$$SR = 4 \times 25 \times 10^{-3} \times 2\pi \times 10^{6} = 0.63\ \text{V}/\mu\text{s}$$

which is the result obtained previously. Observe that Eq. (x5.49) is of the same form as Eq. (13.42), which applies to the two-stage CMOS op amp. Here, $4V_T$ replaces V_{OV}. Since, typically, V_{OV} will be two to three times the value of $4V_T$, a two-stage CMOS op amp with an f_t equal to that of the 741 exhibits a slew rate that is two to three times as large as that of the 741.

EXERCISE

x5.23 Use the value of the slew rate calculated above to find the full-power bandwidth f_M of the 741 op amp. Assume that the maximum output is ±10 V.

Ans. 10 kHz

x5.2 Special Low-Supply-Voltage Performance Requirements

Many special performance requirements stem from the need to operate modern op amps from power supplies of much lower voltages. Thus while the 741-type op amp operated from ±15-V power supplies, many modern BJT op amps are required to operate from a *single power supply of only 2* V *to 3* V. This is done for a number of reasons, including the following:

1. Modern small-feature-size IC fabrication technologies require low power-supply voltages.
2. Compatibility must be achieved with other parts of the system that use low-voltage supplies.
3. Power dissipation must be minimized, especially for battery-operated equipment.

As Fig. x5.19 indicates, there are two important changes: the use of a single ground-referenced power supply V_{CC}, and the low value of V_{CC}. Both of these requirements give rise to changes in performance specifications and pose new design challenges. In the following we discuss two of the resulting changes.

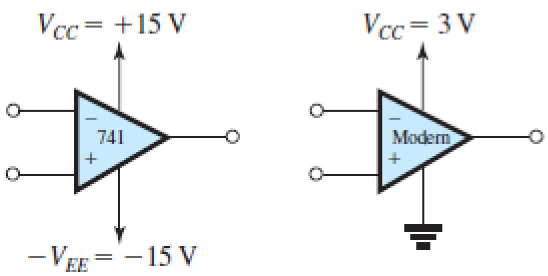

Figure x5.19 Power-supply requirements have changed considerably. Modern BJT op amps are required to operate from a single supply V_{CC} of 2 V to 3 V.

x5.2.1 Rail-to-Rail Input Common-Mode Range

Recall that the input common-mode range of an op amp is the range of common-mode input voltages for which the op amp operates properly and meets its performance specifications, such as voltage gain and CMRR. Op amps of the 741 type operate from ±15-V supplies and exhibit an input common-mode range that extends to within a couple of volts of each supply. Such a gap between the input common-mode range and the power supply is obviously unacceptable if the op amp is to be operated from a single supply that is only 2 V to 3 V. Indeed we will now show that these single-supply, low-voltage op amps need to have an input common-mode range that extends over the entire supply voltage, 0 to V_{CC}, referred to as rail-to-rail input common-mode range.

Consider first the inverting op-amp configuration shown in Fig. x5.20(a). Since the positive input terminal is connected to ground (which is the voltage of the negative supply rail), ground voltage has to be within the allowable input common-mode range. In fact, because for positive output voltages the voltage at the inverting input terminal can go slightly negative, the input common-mode range should extend below the negative supply rail (ground).

Next consider the unity-gain voltage follower obtained by applying 100% negative feedback to an op amp, as shown in Fig. x5.20(b). Here the input common-mode voltage is equal to the input signal v_I. To maximize the usefulness of this buffer amplifier, its input signal v_I should be allowed to extend from 0 to V_{CC}, especially since V_{CC} is only 2 V to 3 V. Thus the input common-mode range should include also the positive supply rail. As shown in Section 13.3.2, modern BJT op amps can operate over an input common-mode voltage range that extends a fraction of a volt beyond its two supply rails: that is, more than rail-to-rail operation!

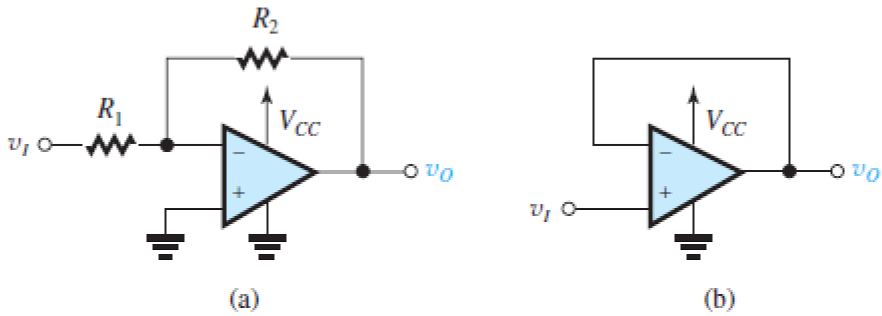

Figure x5.20 **(a)** In the inverting configuration, the positive op-amp input is connected to ground; thus it is imperative that the input common-mode range includes ground voltage. **(b)** In the unity-gain follower configuration, $v_{ICM} = v_I$; thus it is highly desirable for the input common-mode range to include ground voltage and V_{CC}.

x5.2.2 Near Rail-to-Rail Output Signal Swing

In the 741 op amp, we were satisfied with an output that can swing to within 2 Vor so of each of the supply rails. With a supply of ±15 V, this capacity resulted in a respectable ±13-V output range. However, to limit the output swing to within 2 V of the supply rails in an op amp operating from a single 3-V supply would result in an unusable device! Thus, here too, we require near rail-to-rail operation. As shown in Section 13.3.5, this requirement forces us to adopt a whole new approach to output-stage design.