Microelectronic Circuits
8th Edition
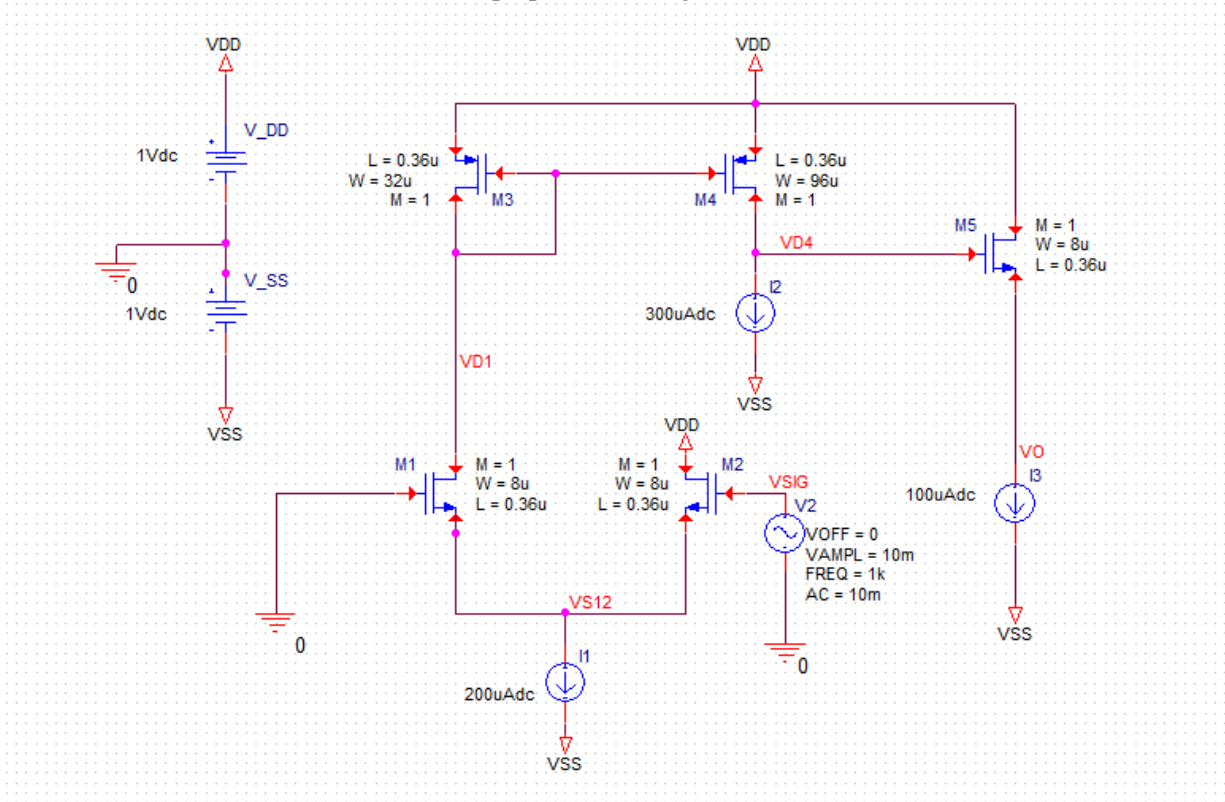
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Spice Problems Solutions
Chapter 11

Prepared by: Nijwm Wary
2019

Problem: 11.37

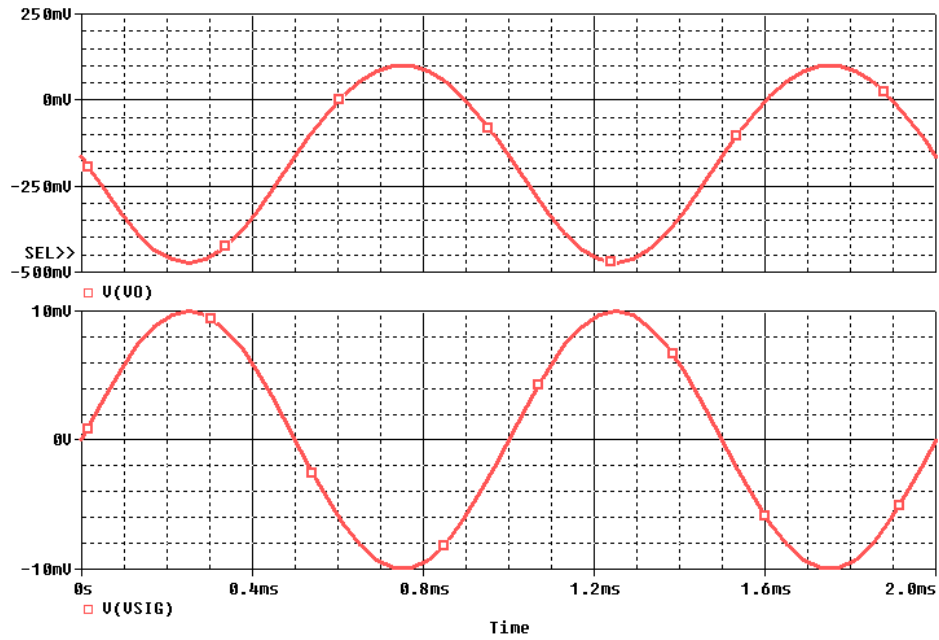1. The schematic with the feedback loop opened at the gate of Q_2 is shown below.

2. Run the netlist and perform operating point analysis. The node voltages are given below.

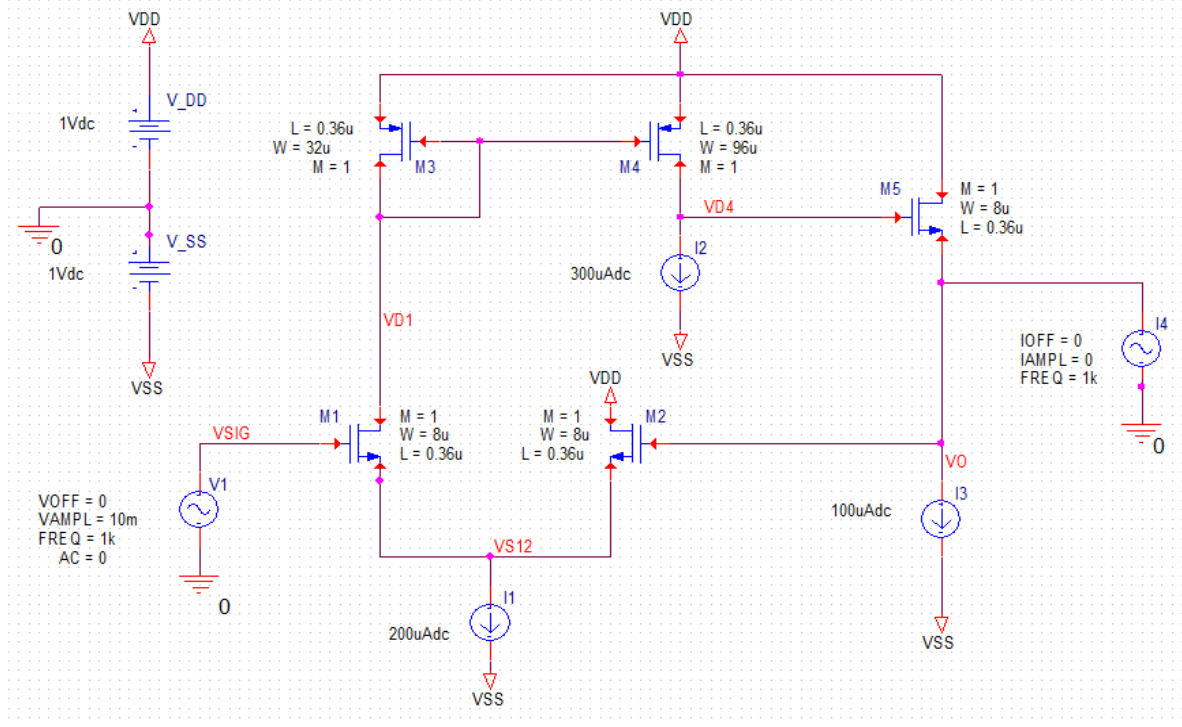| NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE
(VO)	−.1639	(VD1)	.5129	(VD4)	.2895	(VDD)	1.0000
(VSS)	−1.0000	(VS12)	−.4126	(VSIG)	0.0000		

3. The currents, overdrive voltage (VDSAT), g_m , and r_o ($1/g_{ds}$) of the transistors are tabulated by the operating point analysis below.

NAME	M1	M2	M3	M4	M5
MODEL	NMOS0P18	NMOS0P18	PMOS0P18	PMOS0P18	NMOS0P18
ID	9.48E−05	1.05E−04	−9.48E−05	−3.00E−04	1.00E−04
VGS	4.13E−01	4.13E−01	−4.87E−01	−4.87E−01	4.53E−01
VDS	9.25E−01	1.41E+00	−4.87E−01	−7.11E−01	1.16E+00
VBS	4.13E−01	4.13E−01	0.00E+00	0.00E+00	1.64E−01
VTH	2.82E−01	2.82E−01	−3.50E−01	−3.50E−01	3.23E−01
VDSAT	1.30E−01	1.30E−01	−1.37E−01	−1.37E−01	1.30E−01
GM	1.46E−03	1.62E−03	1.38E−03	4.38E−03	1.54E−03
GDS	2.11E−05	2.11E−05	2.34E−05	7.01E−05	2.11E−05

4. Plot V(VSIG) and V(VO) as shown below and find the gain.

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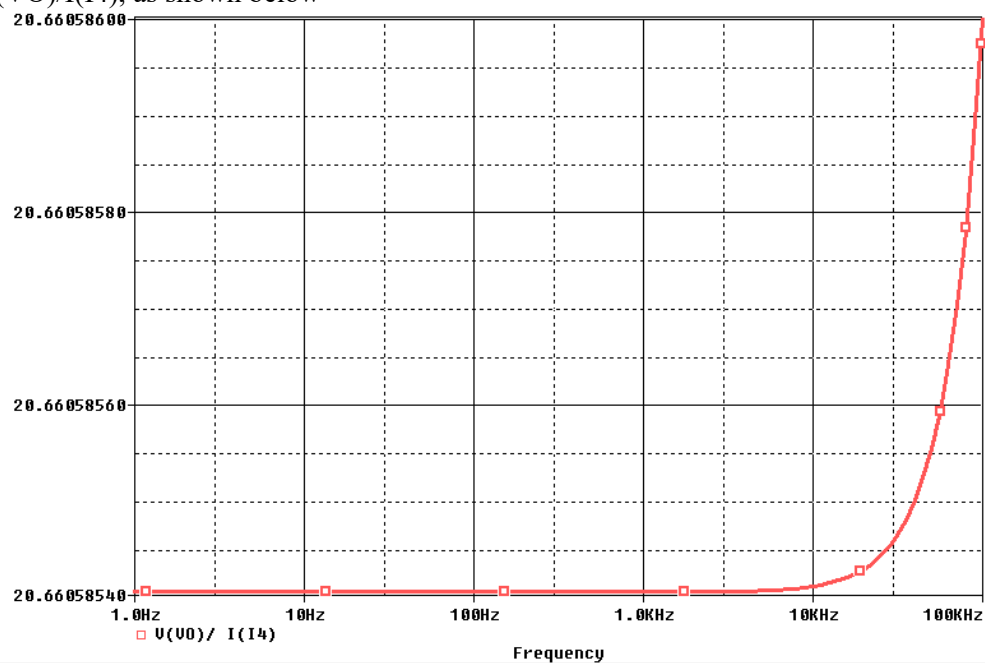*Chapter 11*

5. The gain is -28.7 V/V. This confirms that the feedback is negative.
6. The value of R_o can be calculated from g_{m5} and g_{ds5}. It is $1/g_{m5}||1/g_{ds5}=640 \ \Omega$.
7. The schematic for part (e) of this problem is shown below

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8. Perform a transient analysis and plot V(VO) and V(VSIG) to find the gain. Note that in this case I4 has zero current amplitude.

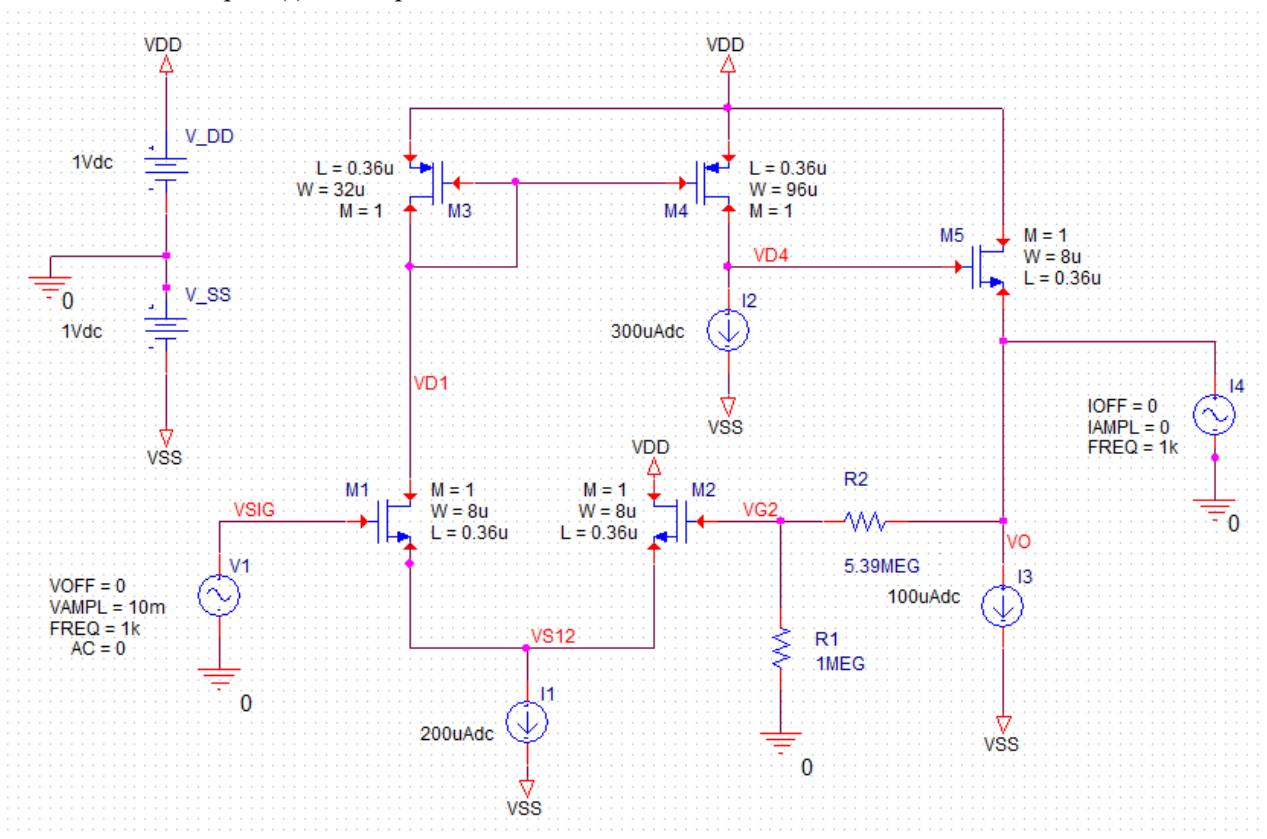
9. The gain is 0.96 V/V.
10. To calculate the output impedance, make the AC amplitude of I4 1Aac and run an AC simulation. Plot V(VO)/I(I4), as shown below

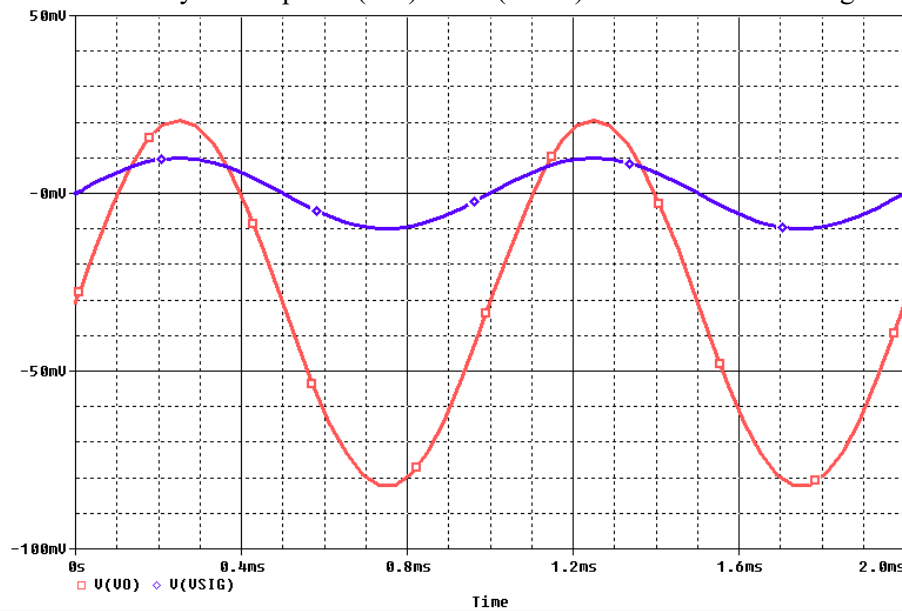11. The output impedance is 20.66 Ω

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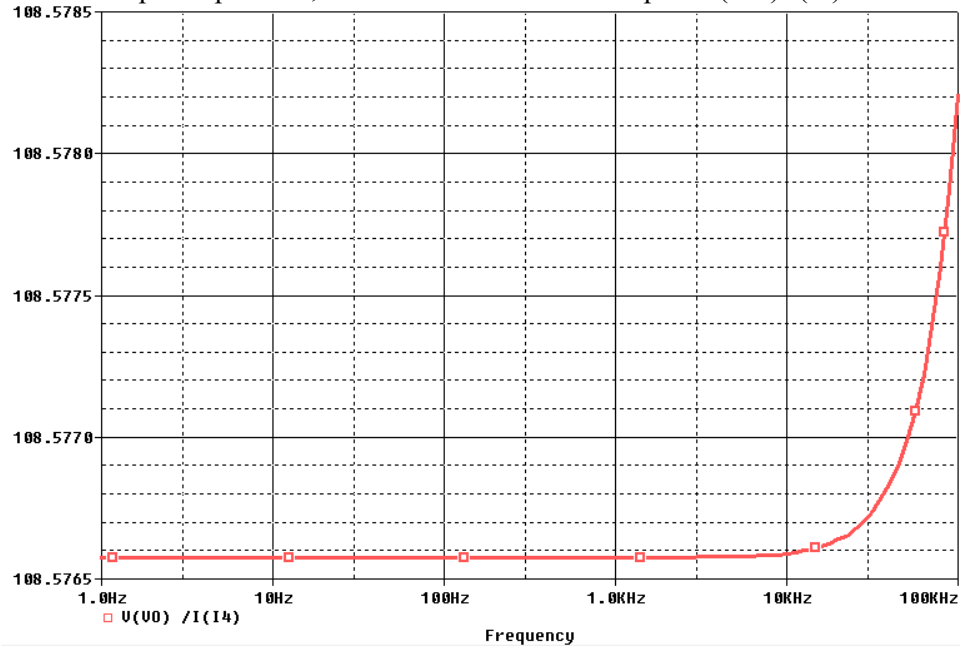12. The schematic for part (f) of this problem is shown below

13. Perform the transient analysis and plot V(VO) and V(VSIG) and find out the new gain.

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14. The gain is 5.13 V/V.
15. To calculate the output impedance, run the AC simulation and plot V(VO)/I(I4)

16. The output impedance is 108.57 Ω.

Netlist:

For part (b) and (c), copy the netlist given below and paste it into a text file and save it with *.cir extension.

```
********Problem: P11_37(b),(c) and (d) ***************
******* Main circuit begins here***************
V_DD        VDD 0 1Vdc
I3          VO VSS DC 100uAdc
I2          VD4 VSS DC 300uAdc
I1          VS12 VSS DC 200uAdc
V_SS         0 VSS 1Vdc
M1          VD1 0 VS12 0 NMOS0P18
+ L=0.36u
+ W=8u
+ M=1
M2          VDD VSIG VS12 0 NMOS0P18
+ L=0.36u
+ W=8u
+ M=1
M3          VD1 VD1 VDD VDD PMOS0P18
+ L=0.36u
```

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```
+ W=32u
+ M=1
M4          VD4 VD1 VDD VDD PMOS0P18
+ L=0.36u
+ W=96u
+ M=1
M5          VDD VD4 VO 0 NMOS0P18
+ L=0.36u
+ W=8u
+ M=1
V2          VSIG 0  AC 10m
+SIN 0 10m 1k 0 0 0
******* Main circuit ends here***************

**************** PMOS model begins here ****************************
*              Level-1 Model for PMOS in model 0.18um CMOS Technology
.model PMOS0P18      PMOS(Level=1 VTO=-0.35 GAMMA=0.3 PHI=0.8
+             LD=0 WD=0 UO=118 LAMBDA=0.28 TOX=4.08E-9 PB=0.9)
**************** PMOS model ends here *****************************************

**************** NMOS model begins here ****************************
*              Level-1 Model for NMOS in model 0.18um CMOS Technology
.model NMOS0P18      NMOS(Level=1 VTO=0.35 GAMMA=0.3 PHI=0.84
+             LD=0 WD=0 UO=473 LAMBDA=0.28 TOX=4.08E-9 PB=0.9)
**************** NMOS model ends here *****************************************

******** Analysis begins here****************
.OP
.TRAN   0.01mS   2mS
.PROBE
.END
******** Analysis ends here****************
```

For part (e), copy the netlist given below and paste it into a text file and save it with *.cir extension.

```
********Problem: P11_37(e) ***************
******* Main circuit begins here**************
V_DD        VDD 0 1Vdc
I3          VO VSS DC 100uAdc
I2          VD4 VSS DC 300uAdc
I1          VS12 VSS DC 200uAdc
V_SS         0 VSS 1Vdc
M1          VD1 VSIG VS12 0 NMOS0P18
+ L=0.36u
+ W=8u
+ M=1
M2          VDD VO VS12 0 NMOS0P18
+ L=0.36u
+ W=8u
+ M=1
M3          VD1 VD1 VDD VDD PMOS0P18
+ L=0.36u
+ W=32u
+ M=1
M4          VD4 VD1 VDD VDD PMOS0P18
+ L=0.36u
+ W=96u
+ M=1
M5          VDD VD4 VO 0 NMOS0P18
+ L=0.36u
+ W=8u
+ M=1
V1          VSIG 0  AC 0
```

```
+SIN 0 10m 1k 0 0 0
I4          VO 0 DC 0Adc AC 1Aac
+SIN 0 0 1k 0 0 0


******* Main circuit ends here***************

***************** PMOS model begins here ******************************
*               Level-1 Model for PMOS in model 0.18um CMOS Technology
.model PMOS0P18      PMOS(Level=1 VTO=-0.35 GAMMA=0.3 PHI=0.8
+           LD=0 WD=0 UO=118 LAMBDA=0.28 TOX=4.08E-9 PB=0.9)
***************** PMOS model ends here ******************************************

***************** NMOS model begins here ******************************
*               Level-1 Model for NMOS in model 0.18um CMOS Technology
.model NMOS0P18      NMOS(Level=1 VTO=0.35 GAMMA=0.3 PHI=0.84
+           LD=0 WD=0 UO=473 LAMBDA=0.28 TOX=4.08E-9 PB=0.9)
***************** NMOS model ends here ******************************************

********* Analysis begins here*****************
.OP
.TRAN   0.01mS   2mS
*.AC   DEC   20   1 100K
.PROBE
.END
********* Analysis ends here*****************
```

For part (f), copy the netlist given below and paste it into a text file and save it with *.cir extension.

```
********Problem: P11_37(f) ****************
******* Main circuit begins here*************
V_DD         VDD 0 1Vdc
I3           VO VSS DC 100uAdc
I2           VD4 VSS DC 300uAdc
I1           VS12 VSS DC 200uAdc
V_SS         0 VSS 1Vdc
M1           VD1 VSIG VS12 0 NMOS0P18
+ L=0.36u
+ W=8u
+ M=1
M2           VDD VG2 VS12 0 NMOS0P18
+ L=0.36u
+ W=8u
+ M=1
M3           VD1 VD1 VDD VDD PMOS0P18
+ L=0.36u
+ W=32u
+ M=1
M4           VD4 VD1 VDD VDD PMOS0P18
+ L=0.36u
+ W=96u
+ M=1
M5           VDD VD4 VO 0 NMOS0P18
+ L=0.36u
+ W=8u
+ M=1
V1           VSIG 0  AC 0
+SIN 0 10m 1k 0 0 0
I4           VO 0 DC 0Adc AC 0Aac
+SIN 0 0 1k 0 0 0
R1           0 VG2  1MEG TC=0,0
R2           VO VG2  5.39MEG TC=0,0
******* Main circuit ends here***************

***************** PMOS model begins here ******************************
```

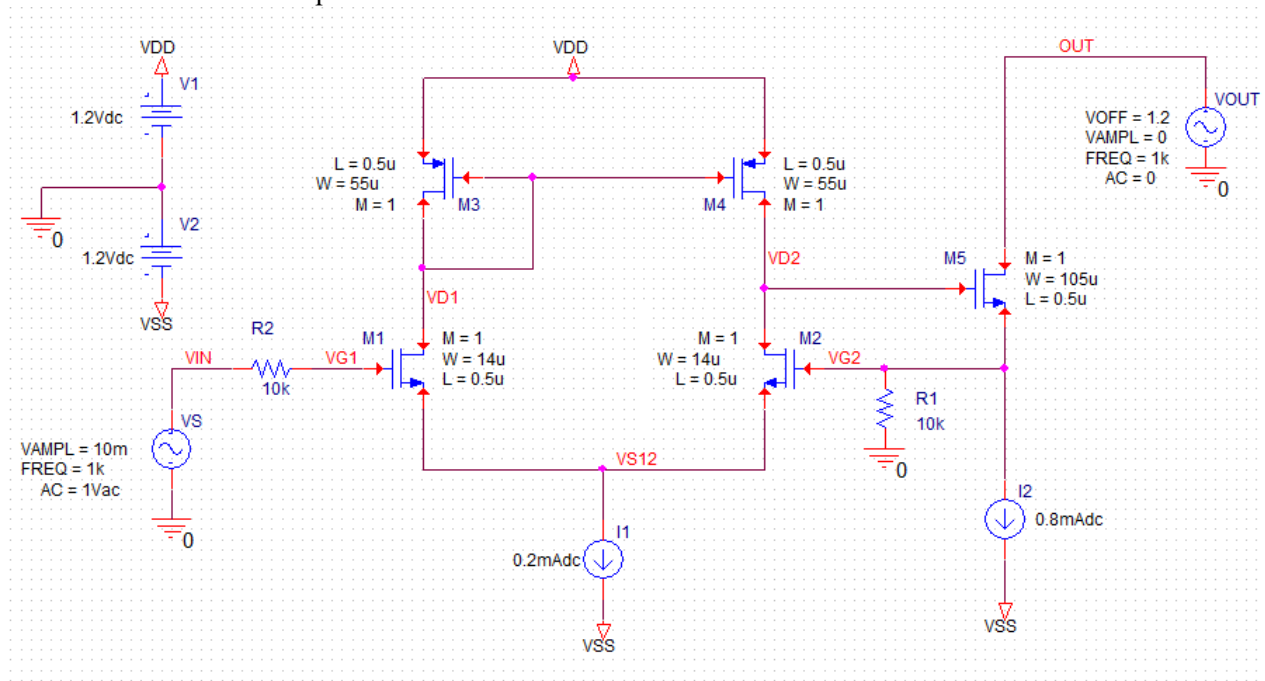*Chapter 11*

```
*              Level-1 Model for PMOS in model 0.18um CMOS Technology
.model PMOS0P18       PMOS(Level=1 VTO=-0.35 GAMMA=0.3 PHI=0.8
+              LD=0 WD=0 UO=118 LAMBDA=0.28 TOX=4.08E-9 PB=0.9)
***************** PMOS model ends here *****************************************

***************** NMOS model begins here ******************************
*              Level-1 Model for NMOS in model 0.18um CMOS Technology
.model NMOS0P18       NMOS(Level=1 VTO=0.35 GAMMA=0.3 PHI=0.84
+              LD=0 WD=0 UO=473 LAMBDA=0.28 TOX=4.08E-9 PB=0.9)
***************** NMOS model ends here *****************************************

******** Analysis begins here*****************
.OP
.TRAN   0.01mS   2mS
*.AC  DEC   20   1 100K
.PROBE
.END
******** Analysis ends here*****************
```

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Problem: 11.58

1. The schematic for this problem is shown below.
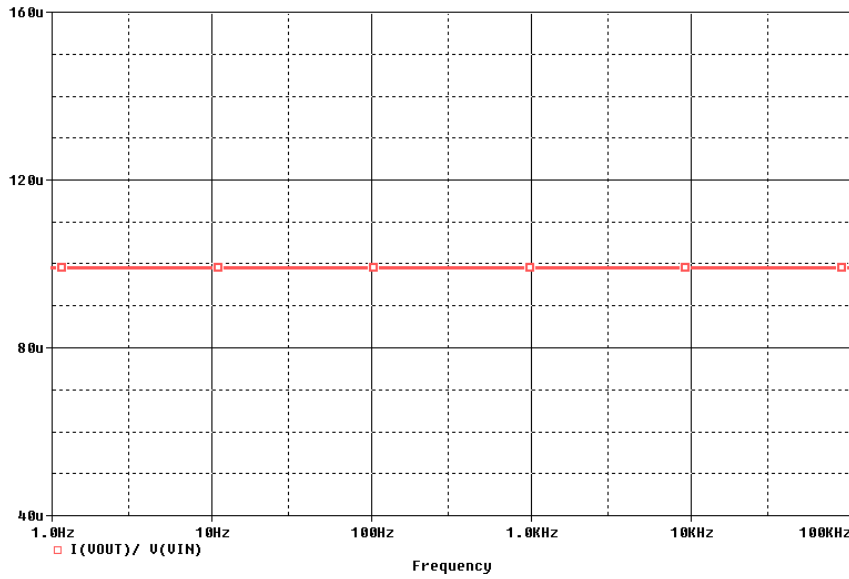

2. For part (a), run the netlist and perform operating point analysis and find out the node voltages and currents.

```
NODE    VOLTAGE      NODE    VOLTAGE      NODE    VOLTAGE      NODE    VOLTAGE

(  OUT)    1.2000  (  VD1)      .5945  (  VD2)      .6072  (  VDD)    1.2000

(  VG1)    0.0000  (  VG2)-122.1E-06  (  VIN)    0.0000  (  VSS)   -1.2000

( VS12)   -.6008
```

```
NAME        M1          M2          M3          M4          M5
MODEL       NMOS0P5     NMOS0P5     PMOS0P5     PMOS0P5     NMOS0P5
ID          1.00E-04    1.00E-04    -1.00E-04   -1.00E-04   8.00E-04
VGS         6.01E-01    6.01E-01    -6.06E-01   -6.06E-01   6.07E-01
VDS         1.20E+00    1.21E+00    -6.06E-01   -5.93E-01   1.20E+00
VBS         0.00E+00    0.00E+00    0.00E+00    0.00E+00    0.00E+00
VTH         4.00E-01    4.00E-01    -4.00E-01   -4.00E-01   4.00E-01
VDSAT       2.01E-01    2.01E-01    -2.06E-01   -2.06E-01   2.07E-01
```

3. For part (c), perform AC analysis and plot I(VOUT)/V(VIN) as shown below.
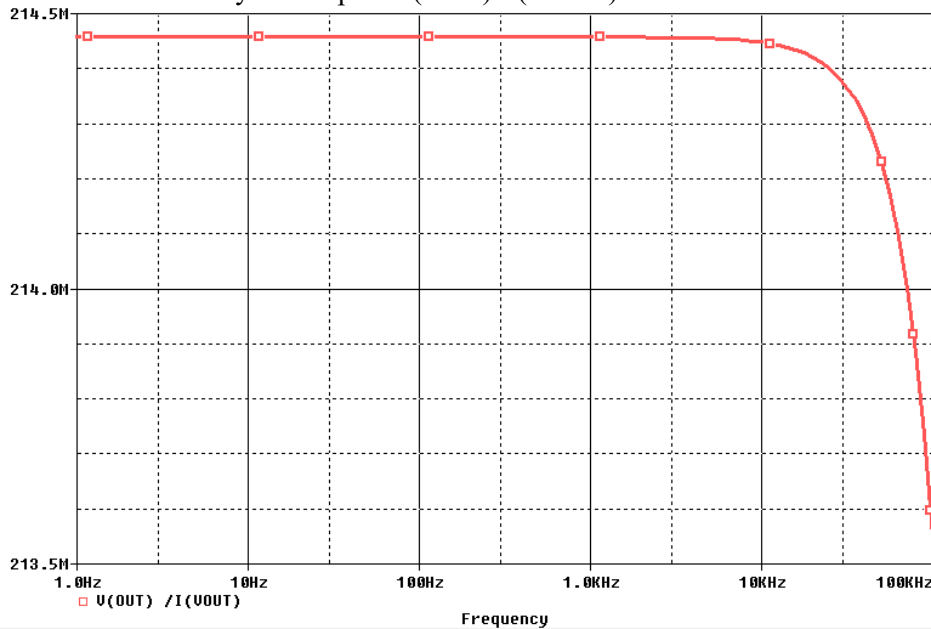

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4. So, A_f is 99 μA/V.

5. For part (d) to calculate the Rout, make the AC amplitude of VS zero and that of VOUT 1Vac as shown below.

```
VS          VIN 0  AC 0Vac
.
.
VOUT            OUT 0  AC 1Vac
```
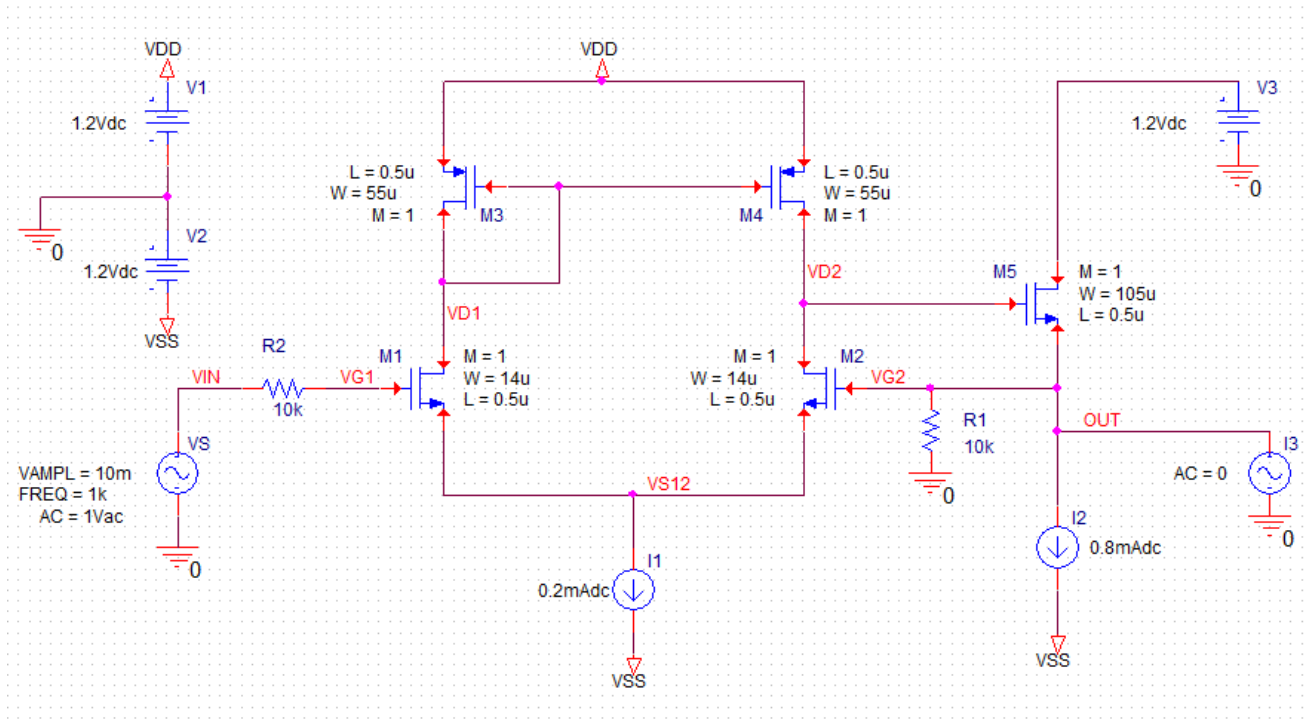
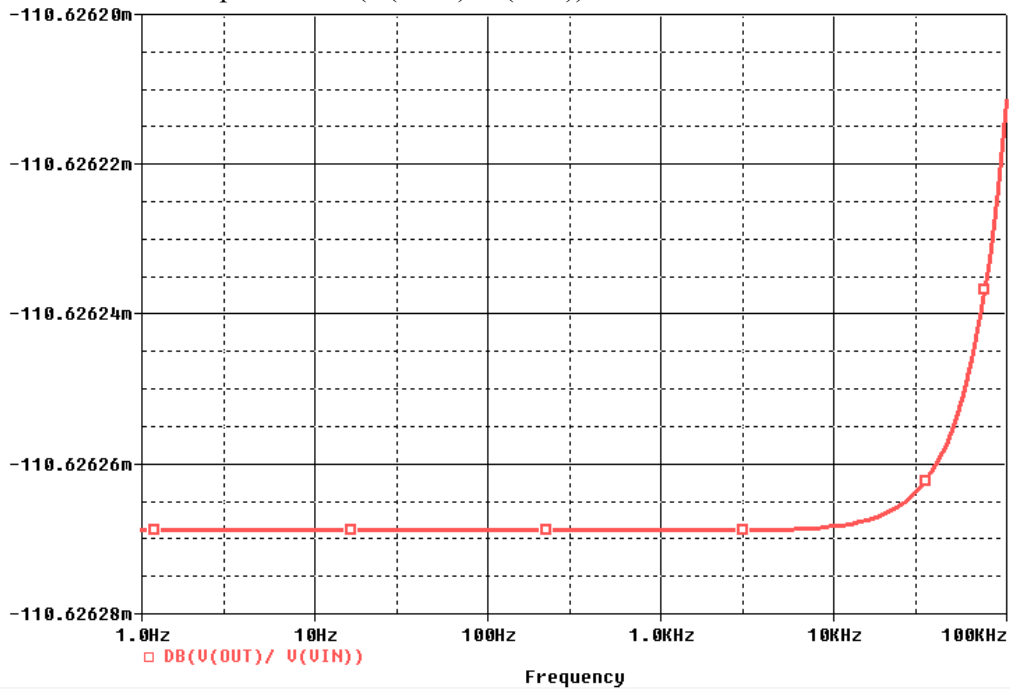6. Perform an AC analysis and plot V(OUT) /I(VOUT) as shown below.

7. So, Rout is 214.4 MΩ.
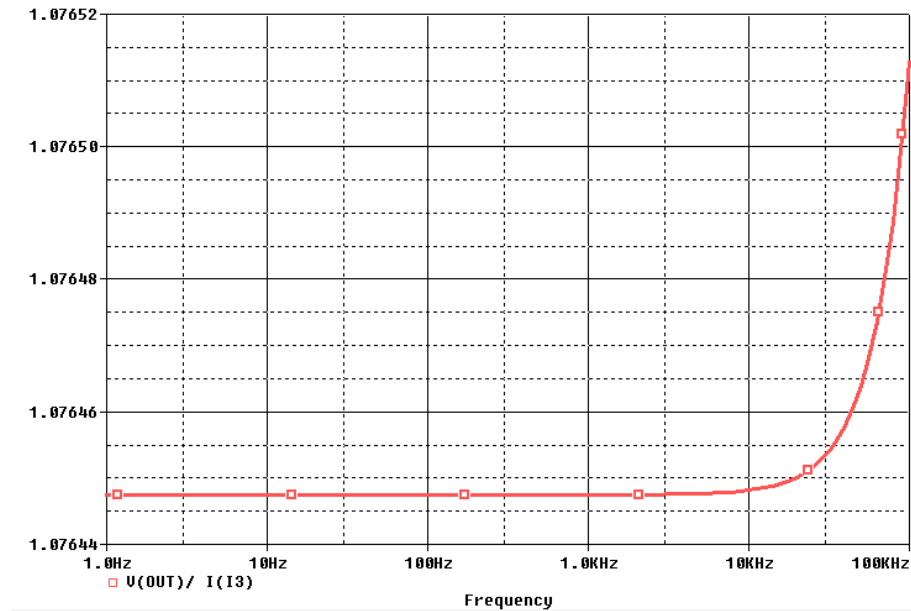
8. The schematic for part (e) is shown below

9. Run the netlist and plot the DB(V(OUT)/ V(VIN)) in dB.

10. The gain is 0.98 V/V

11. Now make the AC amplitude of VS zero and the AC amplitude of I3 as 1. Then run the AC simulation again and plot V(OUT)/I(I3) as shown below

12. The output impedance is 1.07 Ω.

Netlist:

Copy the netlist given below and paste it into a text file and save it with *.cir extension.

```
********Problem: P11_58***************
******* Main circuit begins here**************
M1          VD1 VG1 VS12 VS12 NMOS0P5
+ L=0.5u
+ W=14u
+ M=1
M2          VD2 VG2 VS12 VS12 NMOS0P5
+ L=0.5u
+ W=14u
+ M=1
M3          VD1 VD1 VDD VDD PMOS0P5
+ L=0.5u
+ W=55u
+ M=1
M4          VD2 VD1 VDD VDD PMOS0P5
+ L=0.5u
+ W=55u
+ M=1
I1          VS12 VSS DC 0.2mAdc
M5          OUT VD2 VG2 VG2 NMOS0P5
+ L=0.5u
+ W=105u
+ M=1
I2          VG2 VSS DC 0.8mAdc
```

```
V1          VDD 0 1.2Vdc
V2          0 VSS 1.2Vdc
VS          VIN 0  AC 1Vac
+SIN 0 10m 1k 0 0 0
R1          0 VG2  10k TC=0,0
R2          VG1 VIN  10k TC=0,0
VOUT        OUT 0  AC 0Vac
+SIN 1.2 0 1k 0 0 0

******* Main circuit ends here***************

***************** PMOS model begins here *****************************
.model PMOS0P5 PMOS(Level=1 VTO=-0.4 GAMMA=0.05 PHI=0.8
+           LD=0 WD=0 UO=115 LAMBDA=0.05 TOX=9.5E-9 PB=0.9)
***************** PMOS model ends here ****************************************

***************** NMOS model begins here ****************************
.model NMOS0P5 NMOS(Level=1 VTO=0.4 GAMMA=0.05 PHI=0.8
+           LD=0 WD=0 UO=460 LAMBDA=0.05 TOX=9.5E-9 PB=0.9)
***************** NMOS model ends here ****************************************

******** Analysis begins here*****************
.OP
.AC  DEC   20  1 100K
.PROBE
.END
******** Analysis ends here*****************
```

Copy the netlist given below for part (e) and paste it into a text file and save it with *.cir extension.

```
********Problem: P11_58 (e)***************
******* Main circuit begins here*************
M1          VD1 VG1 VS12 0 NMOS0P5
+ L=0.5u
+ W=14u
+ M=1
M2          VD2 OUT VS12 0 NMOS0P5
+ L=0.5u
+ W=14u
+ M=1
M3          VD1 VD1 VDD VDD PMOS0P5
+ L=0.5u
+ W=55u
+ M=1
M4          VD2 VD1 VDD VDD PMOS0P5
+ L=0.5u
+ W=55u
+ M=1
I1          VS12 VSS DC 0.2mAdc
M5          N16841 VD2 OUT 0 NMOS0P5
+ L=0.5u
+ W=105u
+ M=1
I2          OUT VSS DC 0.8mAdc
V1          VDD 0 1.2Vdc
V2          0 VSS 1.2Vdc
VS          VIN 0  AC 1Vac
+SIN 0 10m 1k 0 0 0
R1          0 OUT  10k TC=0,0
```

```
R2          VG1 VIN  10k TC=0,0
V3          N16841 0 1.2Vdc
I3          OUT 0 DC 0Adc AC 0
+SIN 0 0 1 0 0 0
******* Main circuit ends here***************

***************** PMOS model begins here ******************************
.model PMOS0P5 PMOS(Level=1 VTO=-0.4 GAMMA=0.05 PHI=0.8
+           LD=0 WD=0 UO=115 LAMBDA=0.05 TOX=9.5E-9 PB=0.9)
***************** PMOS model ends here ****************************************

***************** NMOS model begins here ****************************
.model NMOS0P5 NMOS(Level=1 VTO=0.4 GAMMA=0.05 PHI=0.8
+           LD=0 WD=0 UO=460 LAMBDA=0.05 TOX=9.5E-9 PB=0.9)
***************** NMOS model ends here ****************************************

******** Analysis begins here****************
.AC  DEC   20  1 100K
.PROBE
.END
******** Analysis ends here****************
```
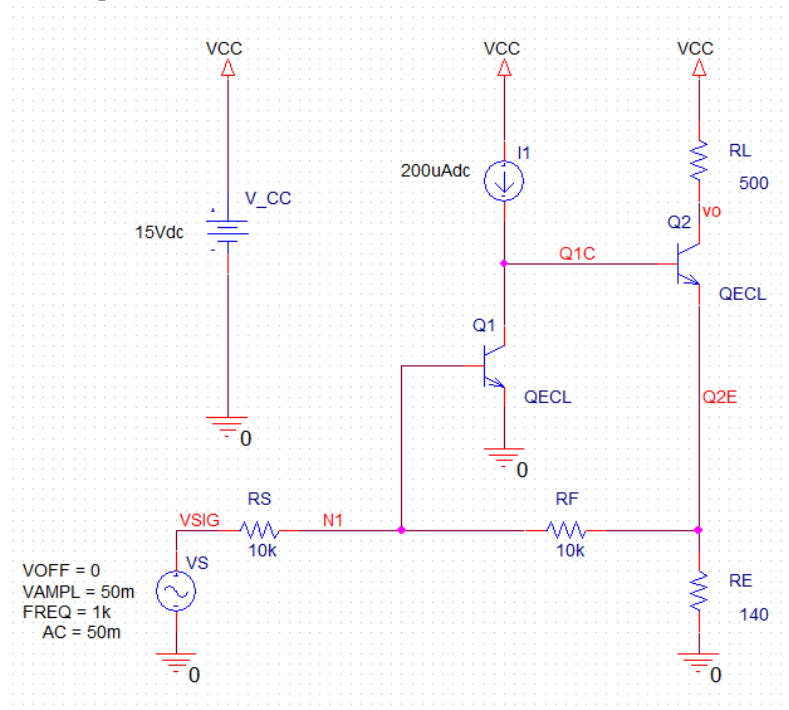
Problem: 11.79

1. The schematic for this problem is shown below

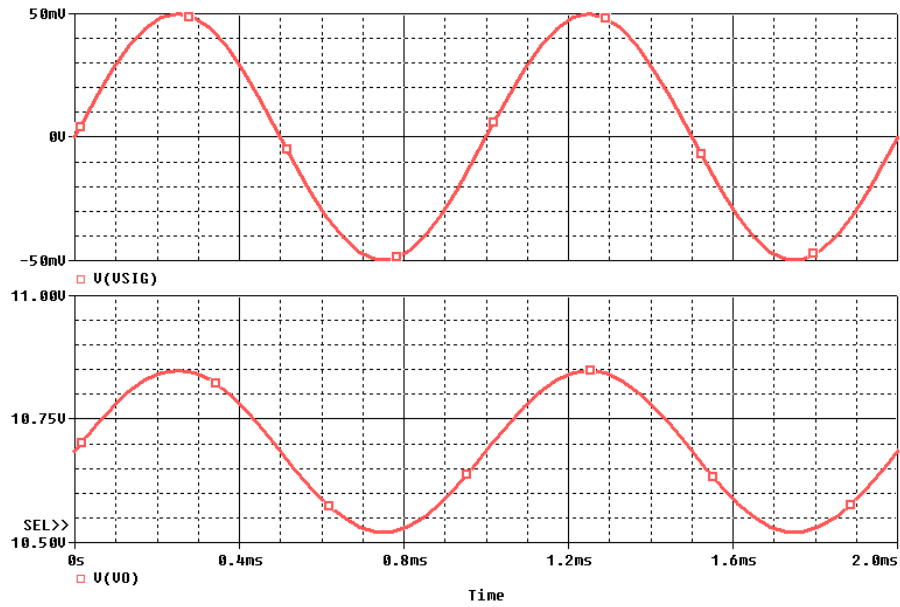2. The node voltages are

```
NODE    VOLTAGE        NODE    VOLTAGE        NODE    VOLTAGE        NODE    VOLTAGE

(   N1)     .6006  (    VO)    10.6840  (   Q1C)     1.9391  (   Q2E)     1.2162
(   VCC)  15.0000  (  VSIG)     0.0000
```

3. The operating conditions of the transistors are

```
NAME           Q1              Q2
MODEL          QECL            QECL
IB             1.51E-06        1.17E-04
IC             8.27E-05        8.63E-03
VBE            6.01E-01        7.23E-01
VBC            -1.34E+00       -8.75E+00
VCE            1.94E+00        9.47E+00
BETADC         5.49E+01        7.36E+01
GM             3.19E-03        3.02E-01
```
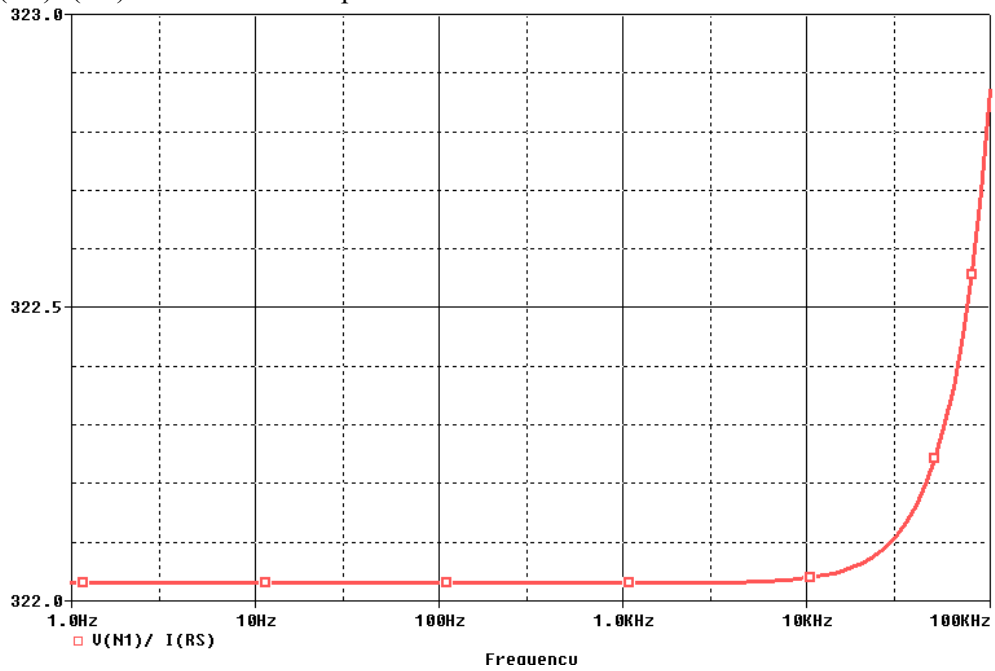
4. Run the transient simulation and plot V(VO) and V(VSIG) to get the gain

5. The gain is 3.3 V/V.
6. Plot V(N1)/I(RS) to calculate the input resistance.

7. The input resistance is 322 Ω.

Netlist:

For part (b) and (c), copy the netlist given below and paste it into a text file and save it with *.cir extension.

```
********Problem: P11_79 ***************
******* Main circuit begins here**************
RS          VSIG N1   10k
RF          N1 Q2E   10k
RE          0 Q2E   140
I1          VCC Q1C DC 200uAdc
RL          VO VCC   500
V_CC         VCC 0 15Vdc
Q1          Q1C N1 0 QECL
Q2          VO Q1C Q2E QECL
VS          VSIG 0   AC 50m
+SIN 0 50m 1k 0 0 0
******* Main circuit ends here**************

************ Model for ECL BJT begins here*****************************
.model QECL    NPN(Is=6.734f Xti=3 Eg=1.11 Vaf=100 Bf=100 Ne=1.259
+              Ise=6.734f Ikf=66.78m Xtb=1.5 Br=.7371 Nc=2 Isc=0 Ikr=0 Rc=1
+              Cjc=3.638p Mjc=.3085 Vjc=0.70 Fc=.5 Cje=4.493p Mje=.2593 Vje=0.70
+              Tr=239.5n Tf=301.2p Itf=.4 Vtf=4 Xtf=2 Rb=10)
************ Model for ECL BJT begins here*****************************

******** Analysis begins here****************
.OP
.TRAN   0.01mS   2mS
*.AC   DEC   20  1 100K
.PROBE
.END
******** Analysis ends here****************
```