Microelectronic Circuits
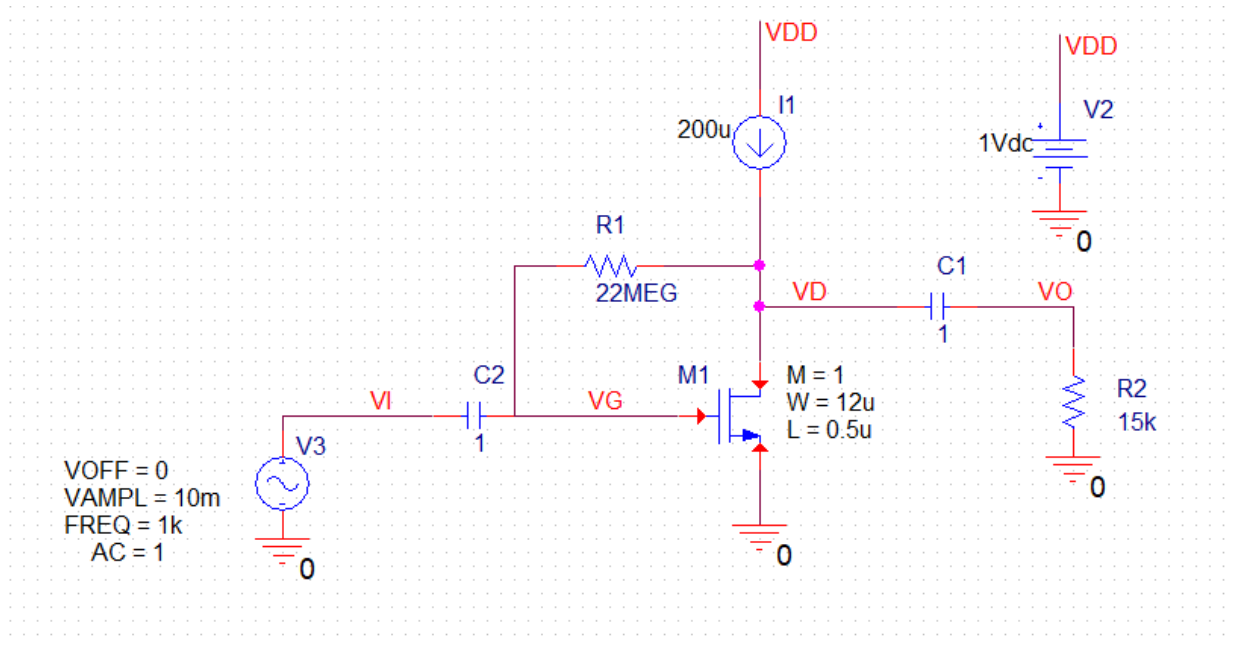# 8th Edition

A. Sedra, K.C. Smith
T. Chan Carusone, V. Gaudet

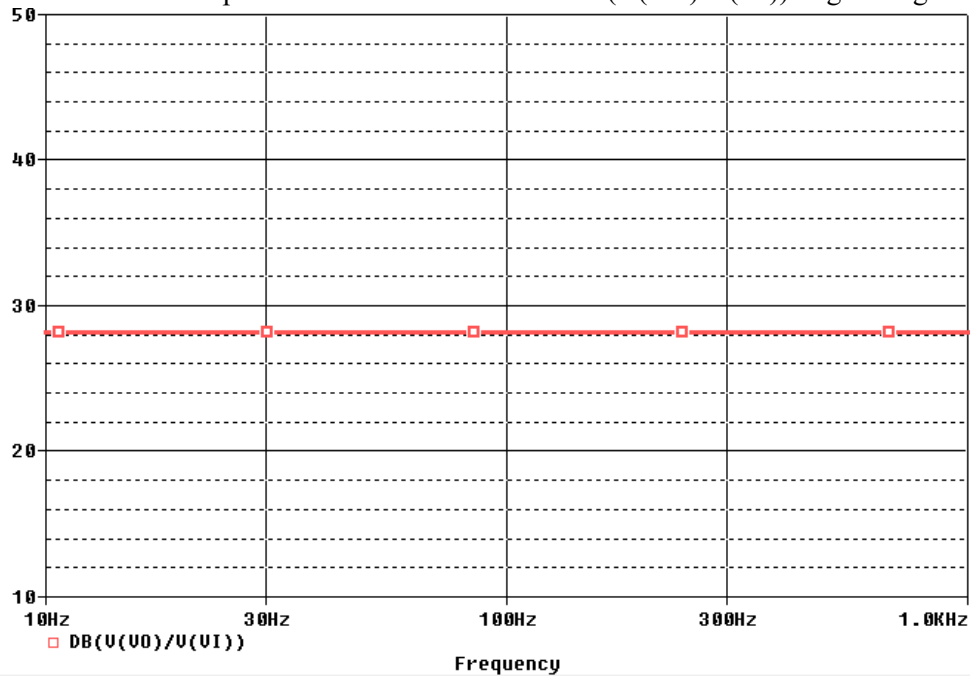*Spice Problems Solutions*
Chapter 7

Prepared by: Nijwm Wary
2019

Problem: 7.31

1. The schematic for this problem is shown below

2. Run the netlist and perform AC simulation. Plot DB(V(VO)/V(VI)) to get the gain.

3. Increase the current I1 to 1mA and plot the waveform again.

Chapter 7

Netlist:

Copy the netlist given below and paste it into a text file and save it with *.cir extension.

```
********Problem: P7_31        ***************
******* Main circuit begins here**************
M1         VD VG 0 0 NMOS0P18
+ L=0.5u
+ W=12u
+ M=1
V2         VDD 0 1Vdc
I1         VDD VD DC 200u
R1         VG VD  22MEG TC=0,0
R2         0 VO  15k TC=0,0
C1         VD VO  1  TC=0,0
C2         VI VG  1  TC=0,0
V3         VI 0  AC 1
+SIN 0 10m 1k 0 0
******* Main circuit ends here**********************************************
**************** NMOS model begins here ****************************************
.model NMOS0P18        NMOS(Level=1 VTO=0.8 GAMMA=0.3 PHI=0.84
+          LD=0 WD=0 UO=450 LAMBDA=0.05 TOX=4.08E-9 PB=0.9)
**************** NMOS model ends here ***************************************

******** Analysis begins here****************
.OP
.AC  DEC   40  10 1K
.PROBE
.END
******** Analysis ends here****************
```
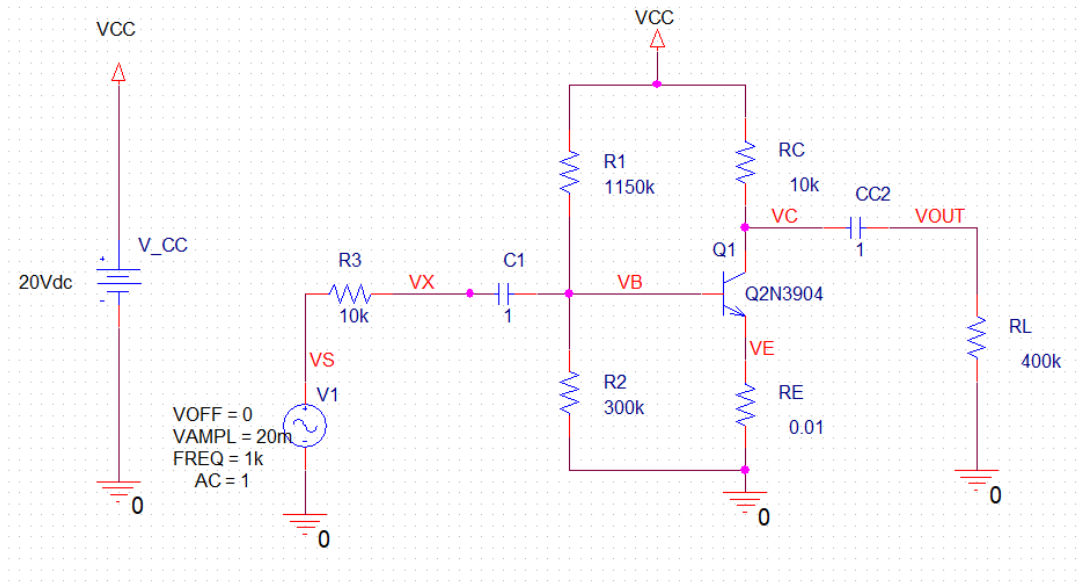
Chapter 7

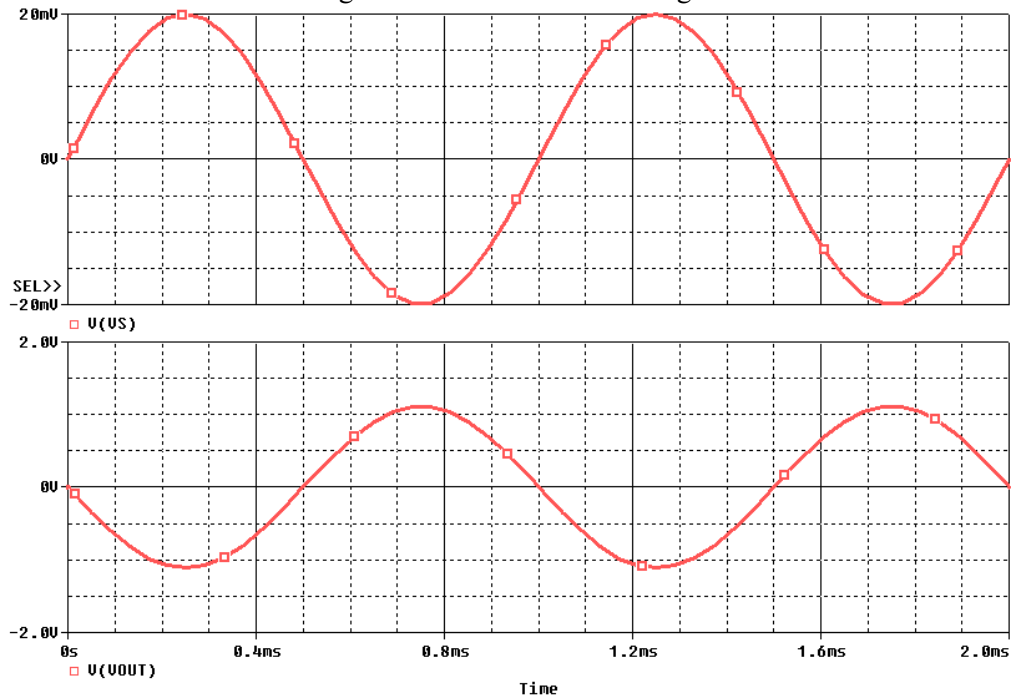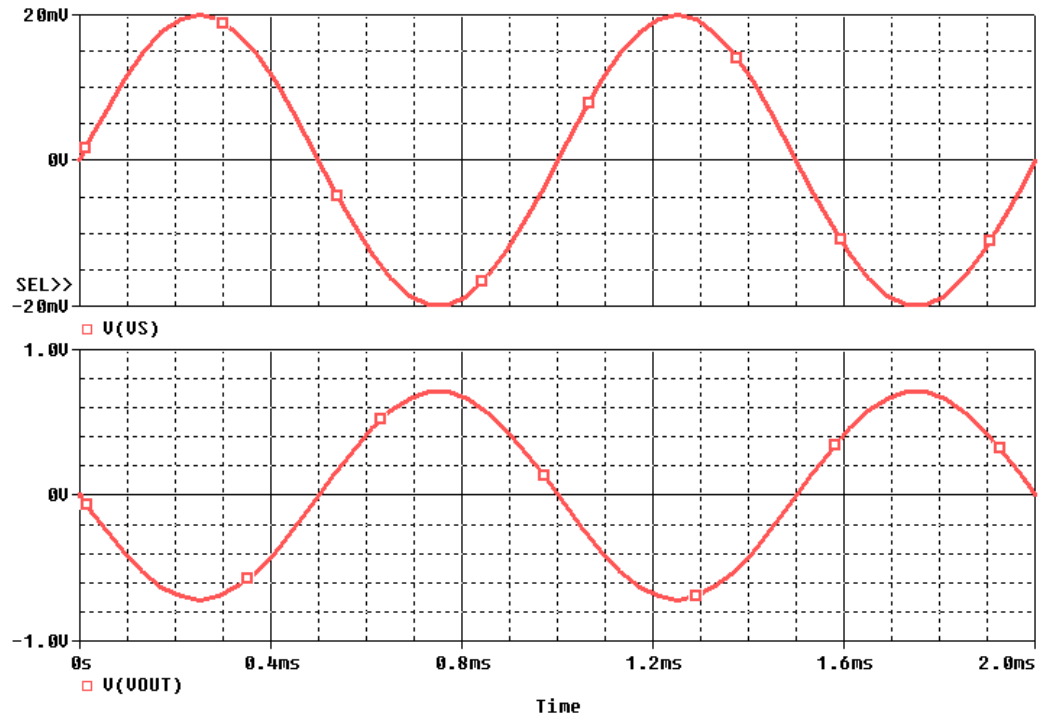## Problem: 7.76
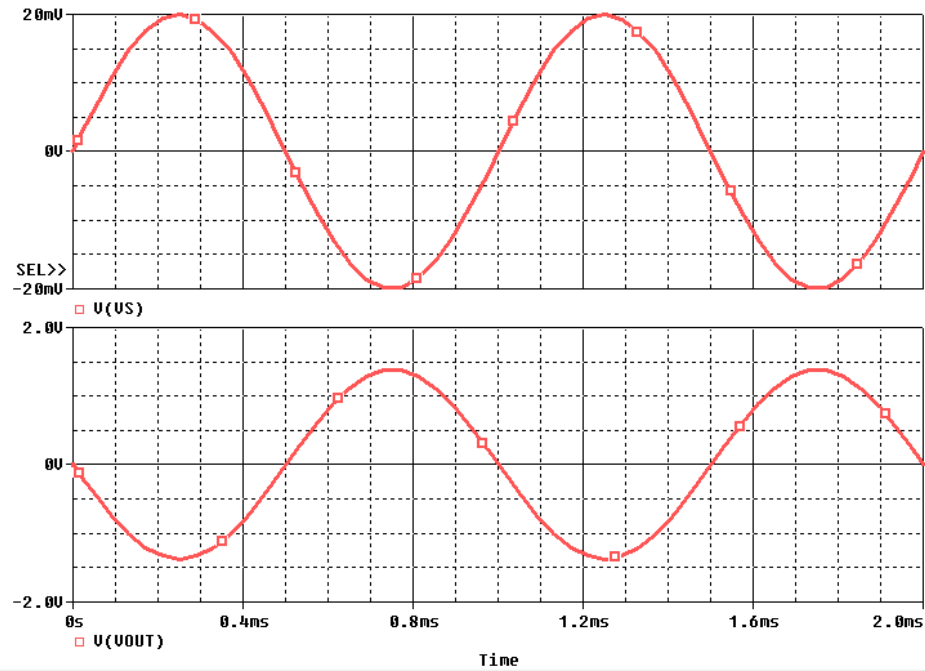
1. The schematics for this problem is shown below

2. Initially, RE is 0.01 Ohms, so practically zero.
3. Plot the VS and VOUT to find the gain. Use cursors to find the gain.

4. To find the variation in gain, change Bf to 50 and 150 and repeat the simulation. VS and VOUT for Bf=50 are shown below

5. VS and VOUT for Bf=150 are shown below

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6. Change RE to 100 Ohms and find the variation in G_v. Find its new nominal value and the expected range by changing Bf to 50 and 150.

Netlist:

Copy the netlist given below and paste it into a text file and save it with *.cir extension.

```
********Problem: P7_76       ***************
******* Main circuit begins here***************

RC          VCC VC  10k
RE          VE 0  0.01
RL          0 VOUT  400k
CC2          VC VOUT  1
V_CC          VCC 0 20Vdc
R1          VB VCC  540k
R2          0 VB  30k
C1          VX VB  1
V1          VS 0  AC 1
+SIN 0 20m 1k 0 0 0
R3          VS VX  10k
Q1          VC VB VE Q2N3904
******* Main circuit ends here*********************************************

**************Model for 2N3904 NPN BJT (from Eval library in Pspice)**********
.model Q2N3904 NPN(Is=6.734f Xti=3 Eg=1.11 Vaf=74.03 Bf=100 Ne=1.259
+           Ise=6.734f Ikf=66.78m Xtb=1.5 Br=.7371 Nc=2 Isc=0 Ikr=0 Rc=1
+           Cjc=3.638p Mjc=.3085 Vjc=.75 Fc=.5 Cje=4.493p Mje=.2593 Vje=.75
+           Tr=239.5n Tf=301.2p Itf=.4 Vtf=4 Xtf=2 Rb=10)
****************Model for 2N3904 NPN BJT

******** Analysis begins here****************
.OP
.Tran 0.01mS 2mS
.Probe
.end
******** Analysis ends here****************
```

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Problem: 7.96

1. The schematic for this problem is shown below
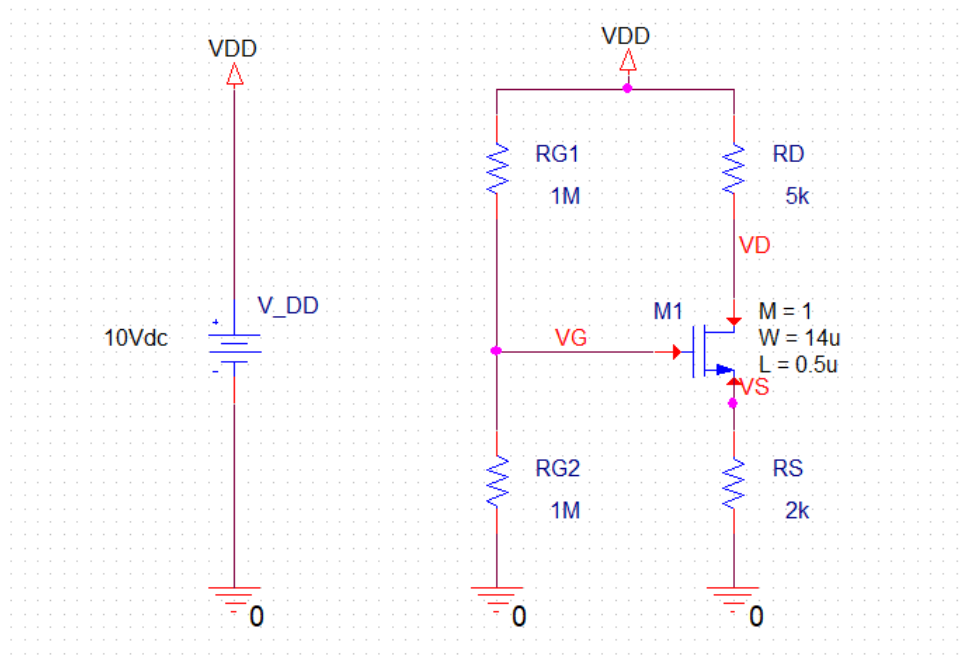
2. The transistor used here has $k_n' = 71.2\ \mu A/V^2$. So, W/L =14μ/0.5μ is chosen to get k_n= 2 mA/V^2.
3. Simulate the netlist and find out the operating voltages.

NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE
(VD)	5.0794	(VG)	5.0000	(VS)	1.9682	(VDD)	10.0000

4. The other operating parameters are

```
NAME        M1
MODEL       NMOS0P5
ID          9.84E-04
VGS         3.03E+00
VDS         3.11E+00
VBS        -1.97E+00
VTH         2.04E+00
VDSAT       9.93E-01
```

5. Change the threshold voltage(VTO) of the NMOS model from 2 to 0.5 and find out the operating voltages and current again.

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Netlist:

Copy the netlist given below and paste it into a text file and save it with *.cir extension.

```
********Problem: P7_96        ***************
******* Main circuit begins here**************
RG2          0  VG   1MEG
V_DD          VDD 0 10Vdc
RS           VS 0   2k
RD           VDD VD   5k
RG1           VDD VG   1MEG
M1           VD VG VS 0 NMOS0P5
+ L=0.5u
+ W=14u
+ M=1
******* Main circuit ends here*******************************


***************** NMOS model begins here ********************
.model NMOS0P5 NMOS(Level=1 VTO=2.0 GAMMA=0.05 PHI=0.8
+           LD=0 WD=0 UO=196 LAMBDA=0 TOX=9.5E-9 PB=0.9 CJ=0.57E-3
+           CJSW=120E-12 MJ=0.5 MJSW=0.4 CGDO=0.4E-9 JS=10E-9 CGBO=0.38E-9
+           CGSO=0.4E-9)
***************** NMOS model ends here *********************

******** Analysis begins here*****************
.op
******** Analysis ends here*******************
```
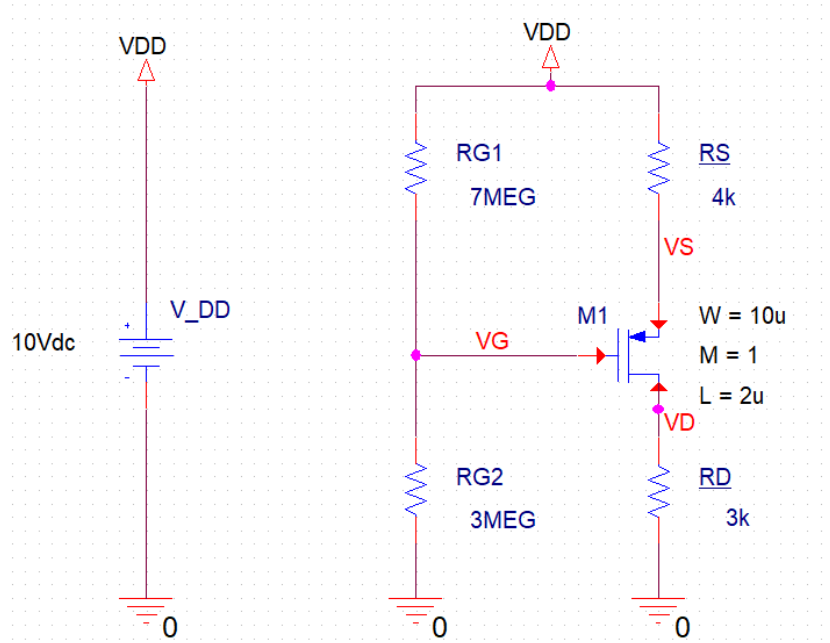
Problem: 7.98

1. The schematic for part (a) of this problem is shown below.

2. The transistor used here has $k_n' = 100$ μA/V^2. So, W/L =10μ/2μ is chosen to get k_n= 0.5 mA/V^2.
3. Simulate the netlist for part (a) and find the operating voltages.

NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE
(VD)	2.9992	(VG)	3.0000	(VS)	6.0010	(VDD)	10.0000

4. The operating point parameters are

```
NAME        M1
MODEL       PMOS0P5
ID          -1.00E-03
VGS         -3.00E+00
VDS         -3.00E+00
VBS          4.00E+00
VTH         -1.06E+00
VDSAT       -1.94E+00
```

5. The schematic for part (b) of this problem is shown below.
6. Here W/L =25μ/2μ is chosen to get k_n= 1.25 mA/V^2.
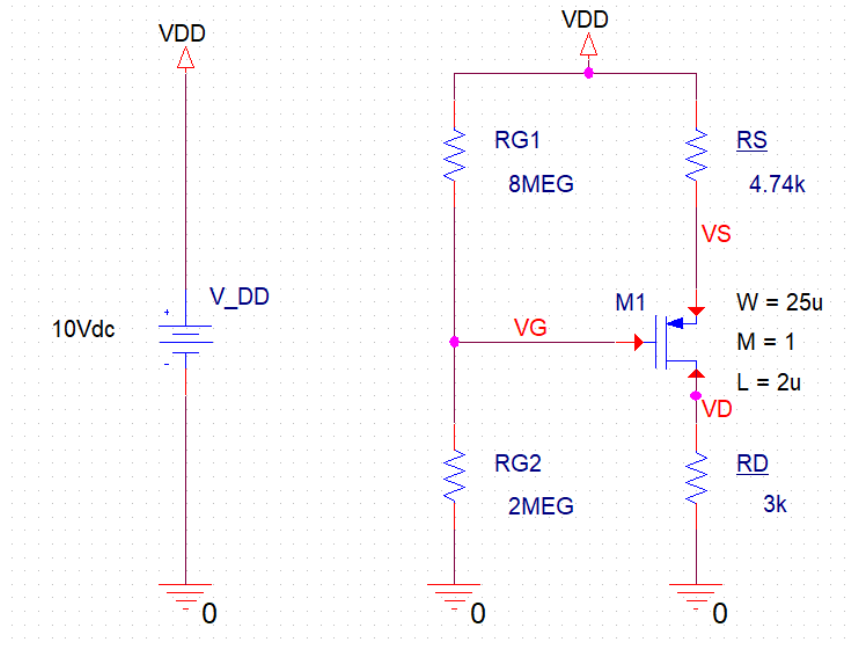
7. Simulate the netlist for part (b) and again find out the operating voltages and currents.

NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE
(VD)	2.9764	(VG)	2.0000	(VS)	5.2972	(VDD)	10.0000

8. The other parameters are

```
NAME        M1
MODEL       PMOS0P5
ID          -9.92E-04
VGS         -3.30E+00
VDS         -2.32E+00
VBS         4.70E+00
VTH         -2.07E+00
VDSAT       -1.23E+00
```

Netlist:

Part (a): Copy the netlist given below and paste it into a text file and save it with *.cir extention.

```
********Problem: P7_98(a)          ***************
******* Main circuit begins here***************
RG2          0 VG   3MEG
V_DD          VDD 0 10Vdc
RD           VD 0   3k
RS           VDD VS   4k
RG1           VDD VG   7MEG
M1           VD VG VS VDD PMOS0P5
+ L=2u
+ W=10u
```

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```
+ M=1
******* Main circuit ends here*******************************

***************** PMOS model begins here ********************
.model PMOS0P5 PMOS(Level=1 VTO=-1 GAMMA=0.045 PHI=0.8
+               LD=0 WD=0 UO=275 LAMBDA=0.02 TOX=9.5E-9 PB=0.9 CJ=0.93E-3
+               CJSW=170E-12 MJ=0.5 MJSW=0.35 CGDO=0.35E-9 JS=5E-9 CGBO=0.38E-9
+               CGSO=0.35E-9)
***************** PMOS model ends here *********************

******** Analysis begins here****************
.op
******** Analysis ends here******************
```

Part (b): Copy the netlist given below and paste it into a text file and save it with *.cir extension.

```
********  Problem: P7_98(b)   ***************
******* Main circuit begins here***************
RG2          0 VG   2MEG
V_DD         VDD 0 10Vdc
RD           VD 0  3k
RS           VDD VS  4.74k
RG1          VDD VG  8MEG
M1           VD VG VS VDD PMOS0P5
+ L=2u
+ W=25u
+ M=1
******* Main circuit ends here*******************************

***************** NMOS model begins here ********************
.model PMOS0P5 PMOS(Level=1 VTO=-2 GAMMA=0.045 PHI=0.8
+               LD=0 WD=0 UO=275 LAMBDA=0.02 TOX=9.5E-9 PB=0.9 CJ=0.93E-3
+               CJSW=170E-12 MJ=0.5 MJSW=0.35 CGDO=0.35E-9 JS=5E-9 CGBO=0.38E-9
+               CGSO=0.35E-9)
***************** NMOS model ends here *********************

******** Analysis begins here****************
.op
******** Analysis ends here******************
```
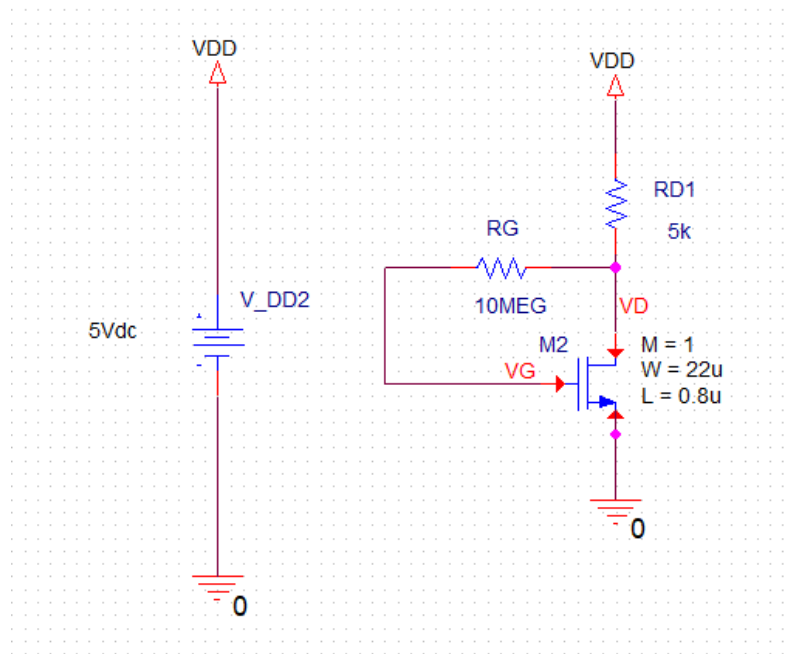
Problem: 7.101

1. The schematic for this problem is shown below

2. The transistor used here has $k_n' = 181.7$ μA/V². So, W/L =22μ/0.8μ is chosen to get k_n=5 mA/V².
3. For part (a), run the netlist and find the voltages.

```
NODE   VOLTAGE       NODE   VOLTAGE       NODE   VOLTAGE       NODE   VOLTAGE

(   VD)   1.2477  (   VG)   1.2477  (   VDD)   5.0000
```

4. For part (b), change the threshold voltage VTO=1.5 V and W=44u

```
NODE   VOLTAGE       NODE   VOLTAGE       NODE   VOLTAGE       NODE   VOLTAGE

(   VD)   1.8545  (   VG)   1.8545  (   VDD)   5.0000
```

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Netlist:

Copy the netlist given below and paste it into a text file and save it with *.cir extension.

```
********Problem: P7_101       ***************
******* Main circuit begins here**************
V_DD         VDD 0 5Vdc
RD           VDD VD  5k
M1           VD VG 0 0 NMOS0P5
+ L=0.8u
+ W=22u
+ M=1
RG           VG VD  10MEG
******* Main circuit ends here******************************
**************** NMOS model begins here ********************
.model NMOS0P5 NMOS(Level=1 VTO=0.7 GAMMA=0.5 PHI=0.8
+             LD=0 WD=0 UO=500 LAMBDA=0.001 TOX=9.5E-9 PB=0.9 CJ=0.57E-3
+             CJSW=120E-12 MJ=0.5 MJSW=0.4 CGDO=0.4E-9 JS=10E-9 CGBO=0.38E-9
+             CGSO=0.4E-9)
**************** NMOS model ends here *********************

******** Analysis begins here****************
.op
******** Analysis ends here******************
```
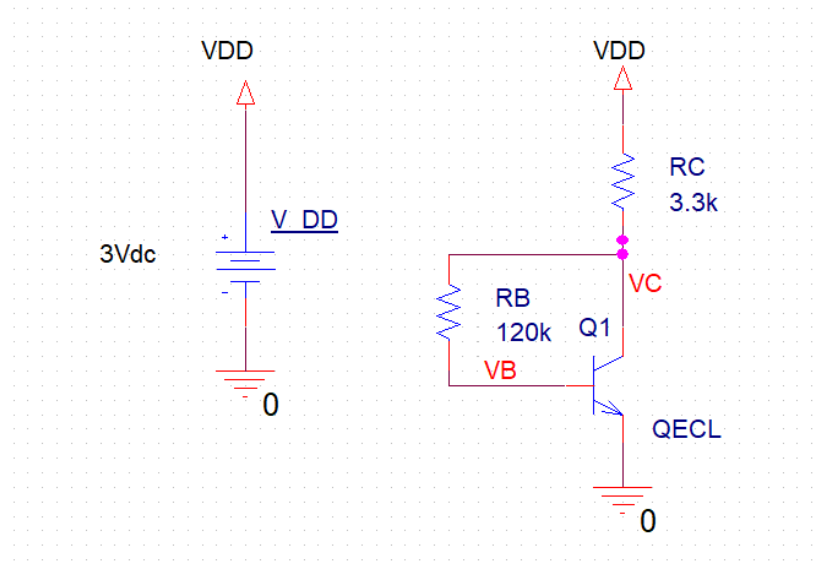
Problem: 7.111

1. The schematic for this problem are shown below.

2. Run the netlist and find the operating voltages.

```
NODE    VOLTAGE      NODE    VOLTAGE      NODE    VOLTAGE      NODE    VOLTAGE

(   VB)     .7315  (    VC)     1.3294  (   VDD)     3.0000
```

3. The currents and other operating point parameters are,

```
NAME        Q1
MODEL       QECL
IB          4.98E-06
IC          5.01E-04
VBE         7.31E-01
VBC         -5.98E-01
VCE         1.33E+00
BETADC      1.01E+02
```

4. Change the value of beta of the transistor to 50 and 150 and find the variation in the operating point.

Netlist:

Copy the netlist given below and paste it into a text file and save it with *.cir extension.

```
********Problem: P7_111        ***************
******* Main circuit begins here**************
Q1           VC VB 0 QECL
RC           VC VDD  3.3k
RB           VB VC   120k
V_DD         VDD 0 3Vdc
******* Main circuit ends here*******************************


************ Model for ECL BJT begins here*******************************
.model QECL    NPN(Is=0.26fA Bf=100 Br=1 Tf=0.1ns Cje=1pF Cjc=1.5pF Va=100)
************ Model for ECL BJT begins here*******************************

******** Analysis begins here*****************
.OP
.END
******** Analysis ends here*****************
```
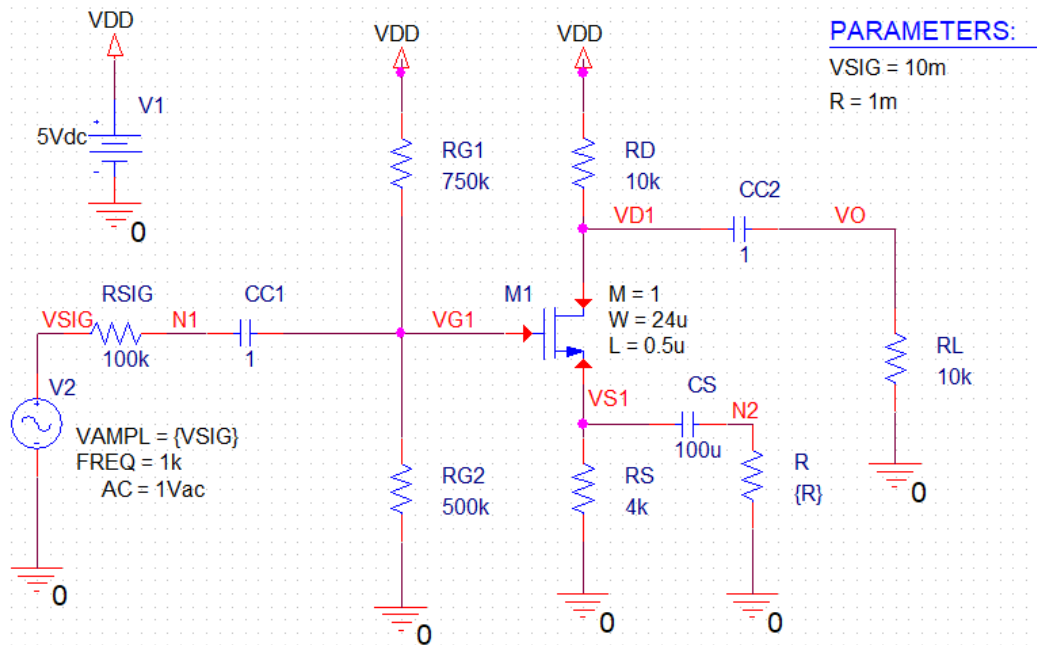
Problem: 7.118

1. The schematic for this problem is shown below.

2. The transistor used here has $k_n' = 167.2 \ \mu A/V^2$. So, W/L =24μ/0.5μ is chosen to get k_n=8 mA/V².

3. For part(a), run the netlist to perform the operating point analysis. The node voltages are,

NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE
(N1)	0.0000	(N2)	0.0000	(VO)	0.0000	(VD1)	2.5398
(VDD)	5.0000	(VG1)	2.0000	(VS1)	.9841	(VSIG)	0.0000

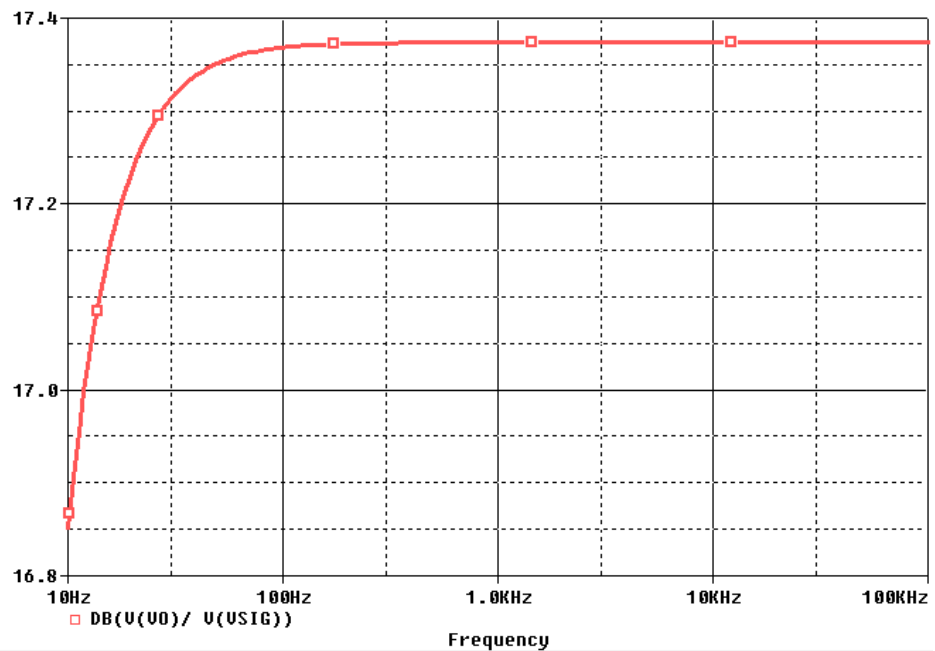4. The operating current is

```
NAME          M1
MODEL         NMOS0P5
ID            2.46E-04
VGS           1.02E+00
VDS           1.56E+00
VBS           -9.84E-01
VTH           7.72E-01
VDSAT         2.44E-01
```
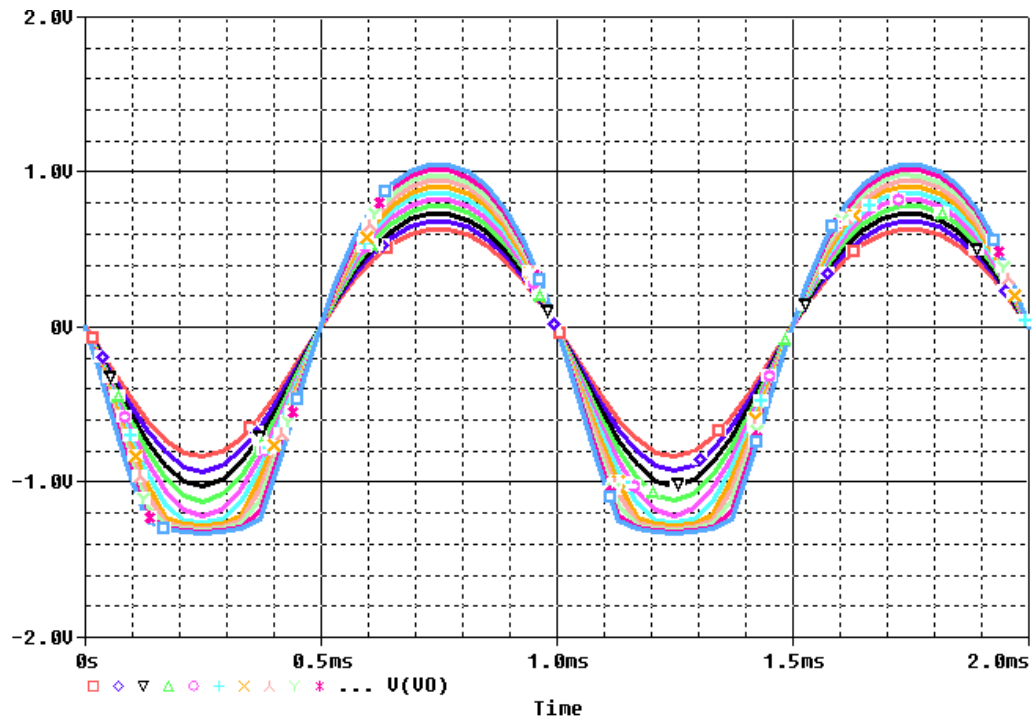
5. For part (b), uncomment the AC analysis and plot V(VG1)/I(CC1) to get the input impedance.

V(VG1)/I(CC1)
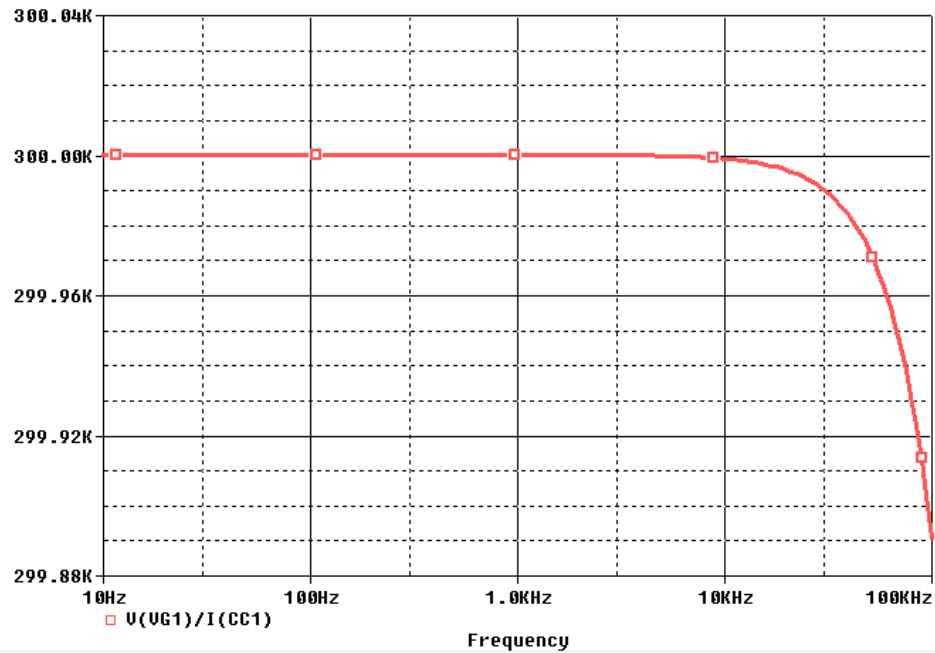
6. To find the gain plot DB(V(VO)/ V(VSIG)).

DB(V(VO)/ V(VSIG))

7. For part (c), uncomment the corresponding parametric transient analysis and plot V(VO) as shown below. Find the input voltage for which the output starts saturating.

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8. The output starts to saturate when input has an amplitude above 0.15 V.
9. For part (d), uncomment the corresponding parametric transient analysis and set VSIG to 300m in the beginning of the netlist as shown below

   ```
   .PARAM   VSIG=300m R=1m
   ```

10. Plot V(VO) as shown below and find the value of R for which the output starts saturating.

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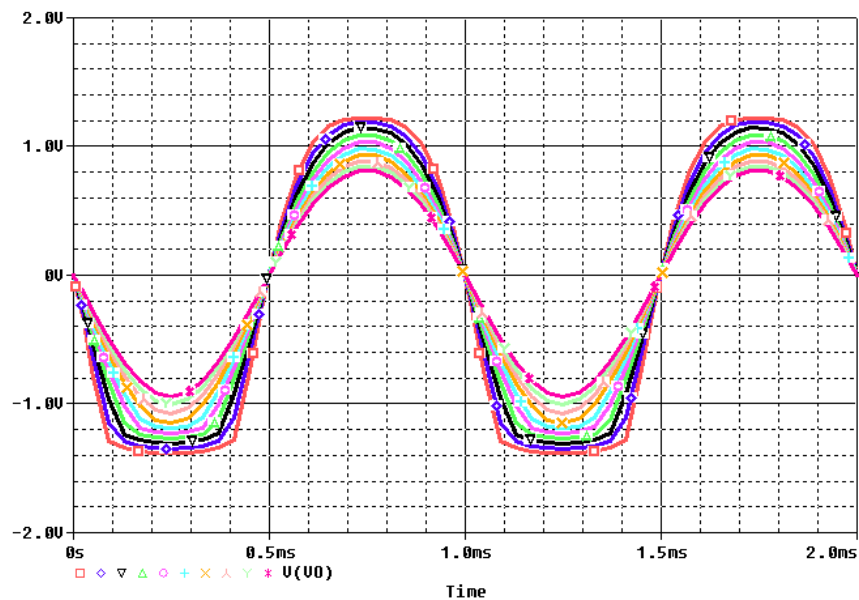
11. The value of the resistor is 500 Ω.

Netlist:

Copy the netlist given below and paste it into a text file and save it with *.cir extension.

```
********Problem: P7_118            ***************
******* Main circuit begins here***************
M1         VD1 VG1 VS1 0 NMOS0P5
+ L=0.5u
+ W=18u
+ M=1
RD         VD1 VDD  10k TC=0,0
RG1         VG1 VDD  750k TC=0,0
RG2          0 VG1  500k TC=0,0
RS          0 VS1   4k TC=0,0
V1         VDD 0 5Vdc
V2         VSIG 0  AC 1Vac
+SIN 0 {VSIG} 1k 0 0 0
R_RSIG        VSIG N1  100k TC=0,0
CC1         N1 VG1   1   TC=0,0
R_RL         0 VO   10k TC=0,0
CC2         VD1 VO   1   TC=0,0
CS         VS1 N2  100u  TC=0,0
R          0 N2   {R} TC=0,0
.PARAM  VSIG=10m R=1m
******* Main circuit ends here***************

**************** NMOS model begins here ****************************
.model NMOS0P5 NMOS(Level=1 VTO=0.75 GAMMA=0.05 PHI=0.8
+             LD=0 WD=0 UO=460 LAMBDA=0.02 TOX=9.5E-9 PB=0.9 CJ=0.57E-3
+             CJSW=120E-12 MJ=0.5 MJSW=0.4 CGDO=0.4E-9 JS=10E-9 CGBO=0.38E-9
+             CGSO=0.4E-9)
**************** NMOS model ends here *****************************************

******** Analysis begins here****************

******Part (a)*********
.op
*********************

******Part (b) *********
*.AC  DEC   40  10 100K
*.PROBE
*.END
*********************

******Part (c)*********
*.TRAN  0.01mS   2mS
*.STEP LIN PARAM vsig 100m 200m 10m
*.PROBE
*.END
*********************

******Part (d)*********
*.TRAN  0.01mS   2mS
*.STEP LIN PARAM R 1m 1k 100
*.PROBE
*.END
*********************

******** Analysis ends here****************
```
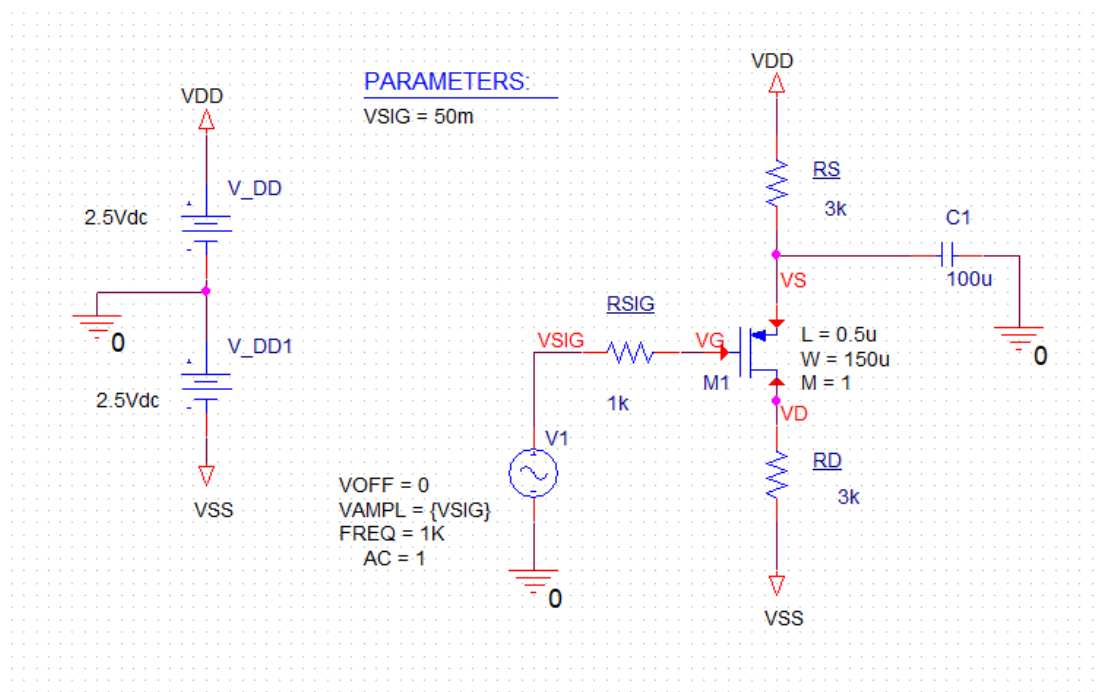
Problem: 7.119

1. The schematic for this problem is shown below.

2. For part (a), run the netlist and find the operating point.

```
NODE    VOLTAGE      NODE    VOLTAGE      NODE    VOLTAGE      NODE    VOLTAGE

(   VD)    -.9970  (    VG)    0.0000  (    VS)     .9970  (   VDD)    2.5000

(  VSS)   -2.5000  ( VSIG)    0.0000
```

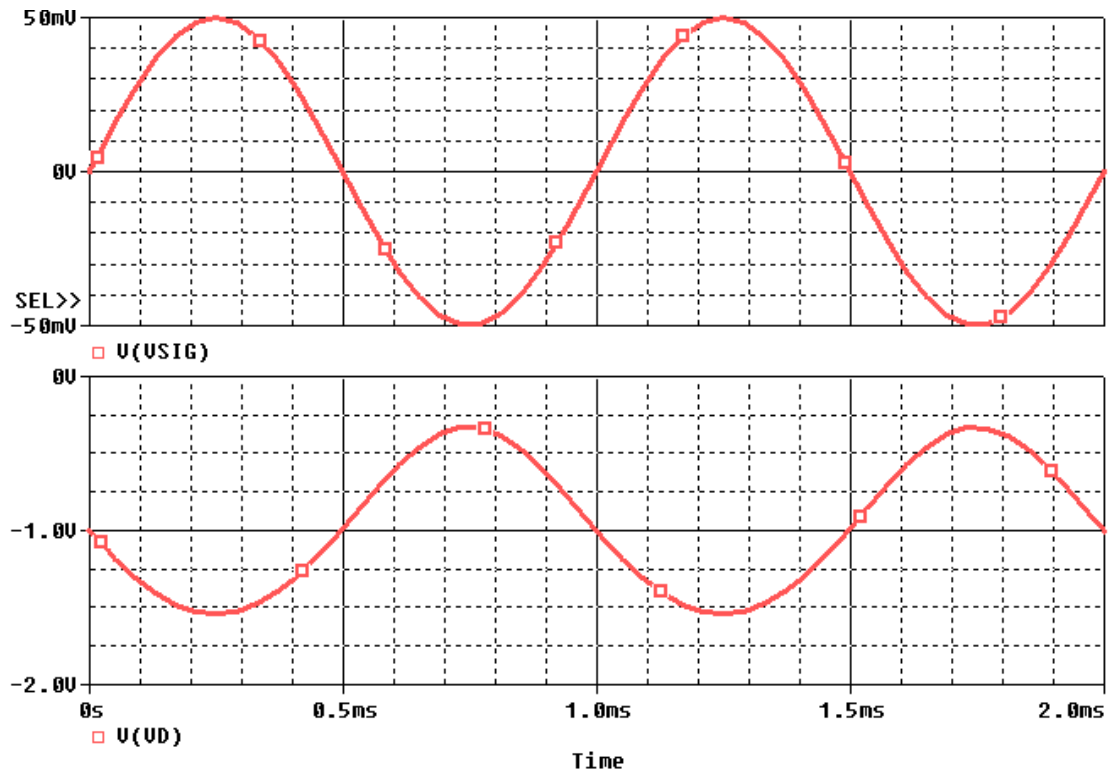3. The operating current is

```
NAME         M1
MODEL        PMOSOP5
ID           -5.01E-04
VGS          -9.97E-01
VDS          -1.99E+00
VBS           0.00E+00
VTH          -7.50E-01
VDSAT        -2.47E-01
```
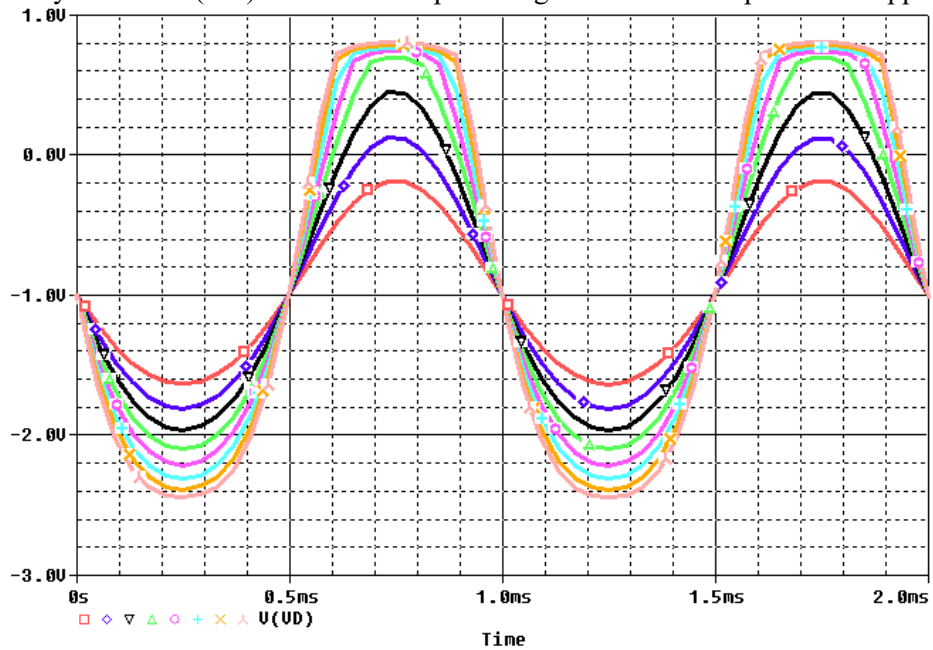
4. For part (b), uncomment the corresponding transient analysis and comment the other analyses. Plot V(D) and V(VSIG).

5. The gain is 12 V/V.
6. For part (c), uncomment the corresponding analysis to sweep the input amplitude and comment the other analyses. Plot V(VD) and find the input swing at which the output starts clipping.

7. For part (d), uncomment the corresponding analysis and comment the other analyses. Increase the resistance of RD and find the at which the output starts clipping. Using this new value of RD, find the gain.

Netlist:

Copy the netlist given below and paste it into a text file and save it with *.cir extension.

```
********Problem: P7_119              ***************
******* Main circuit begins here**************
RSIG        VG VSIG  1k
V_DD         VDD 0 2.5Vdc
RD          VD VSS  3k
RS          VDD VS  3k
V1          VSIG 0  AC 1
+SIN 0 {VSIG} 1K 0 0 0
C1          VS 0  100u
V_DD1        0 VSS 2.5Vdc
M1          VD VG VS VDD PMOS0P5
+ L=0.5u
+ W=150u
+ M=1
.PARAM  vsig=50m

******* Main circuit ends here*******************
**************** NMOS model begins here *****************
.model PMOS0P5 PMOS(Level=1 VTO=-0.75 GAMMA=0.045 PHI=0.8
+             LD=0 WD=0 UO=150 LAMBDA=0.002 TOX=9.5E-9 PB=0.9 CJ=0.93E-3
+             CJSW=170E-12 MJ=0.5 MJSW=0.35 CGDO=0.35E-9 JS=5E-9 CGBO=0.38E-9
+             CGSO=0.35E-9)

**************** NMOS model ends here ******************

******** Analysis begins here****************
******Part (a)*********
.op
*********************

******Part (b) and part (d)*********
*.TRAN  0.01mS  2mS
*.PROBE
*.END
*********************

******Part (c)*********
*.TRAN  0.01mS  2mS
*.STEP LIN PARAM vsig 60m 200m 20m
*.PROBE
*.END
*********************

******** Analysis ends here******************
```