Microelectronic Circuits
8th Edition

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Spice Problems Solutions
Chapter 2

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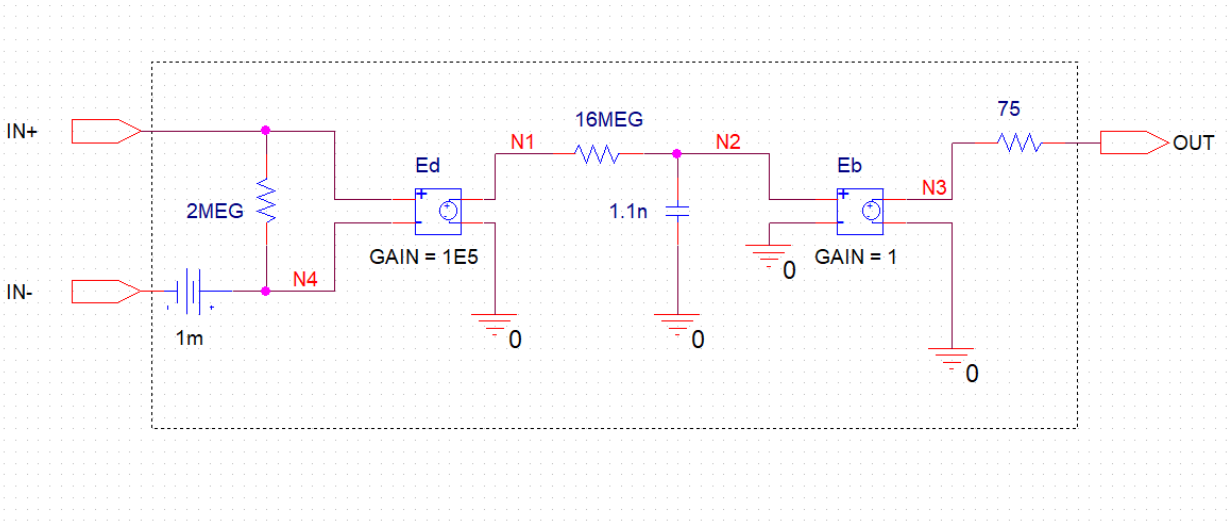
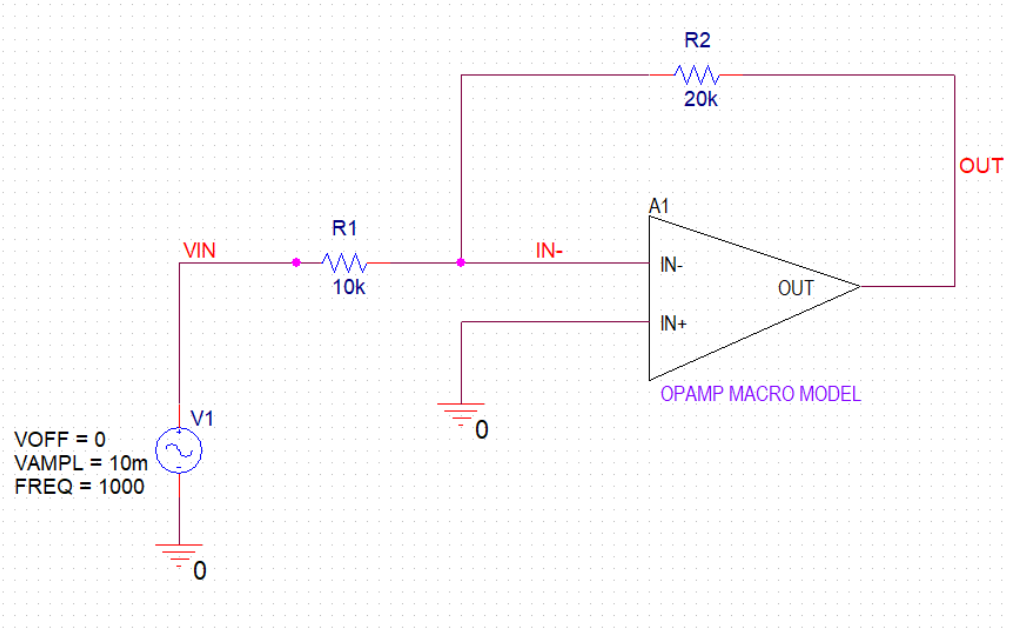
2019

Problem: 2.12

1. The macro model for the opamp used in this problem is shown below

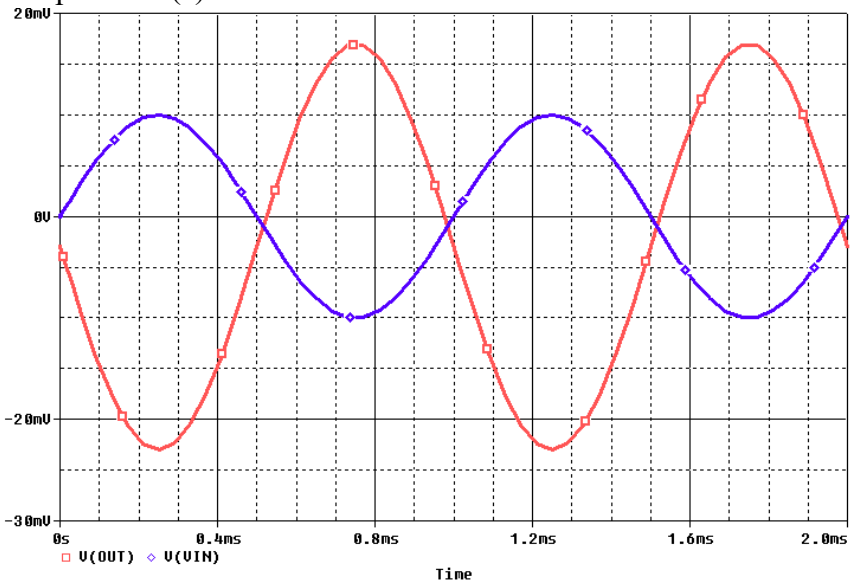


2. The schematic for this problem is shown below



3. Enter the values of R1 and R2 as required by each part of the problem (a,b,c,d,e).
4. Do not change the source frequency or amplitude of V1 which have been chosen so that the op amp behaves ideally.
5. Run the netlist file to perform transient analysis and plot V(OUT) and V(VIN).

6. The plot for problem (a) where R1=10 kΩ and R2=20 kΩ is shown below.



7. Use cursors to measure the peak-to-peak voltage of the output and input. Divide these quantities to get the gain.
8. Change the values of R1 and R2 for parts (b,c,d,e) of the problem and observe the gain.

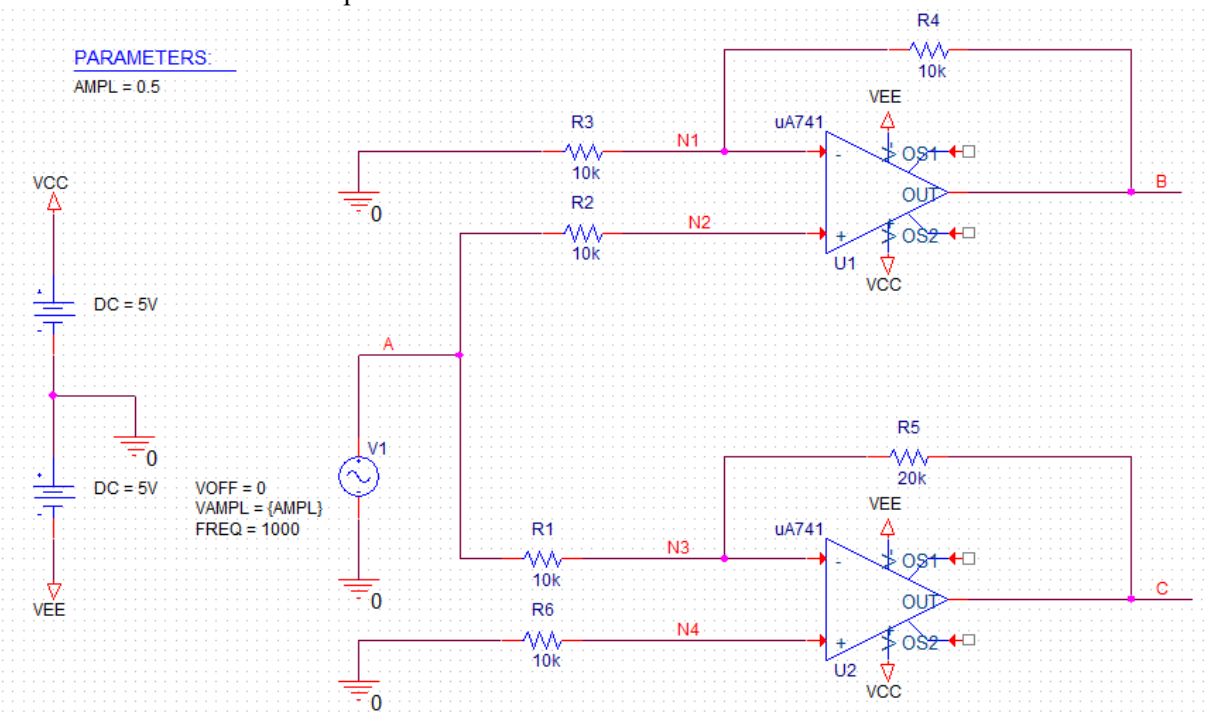
Netlist:

Copy the netlist given below and paste it into a text file and save it with *.cir extension.

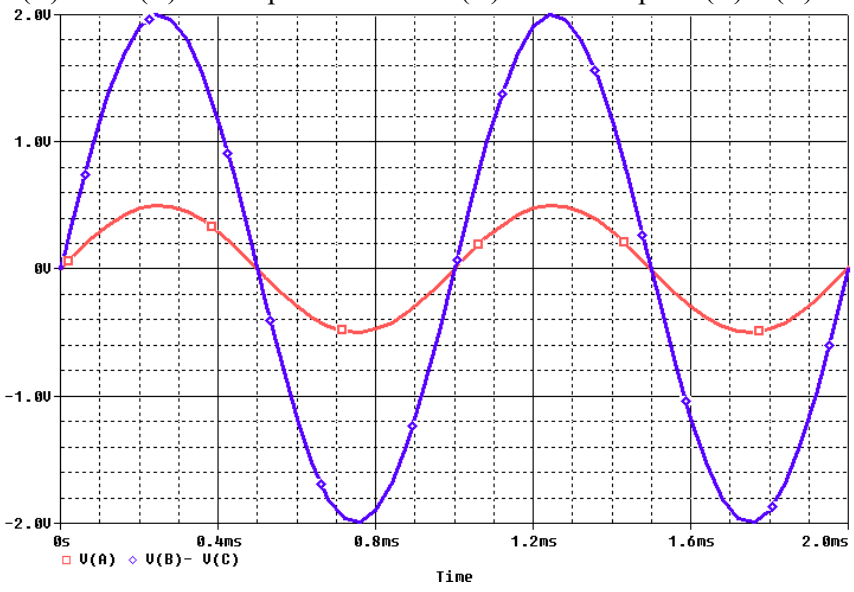
```
********Problem: P2_12         ***************
******* Main circuit begins here**************
R1          VIN IN-  10k
R2          IN- OUT  20k
V1          VIN 0
+SIN 0 10m 1000 0 0 0
X_A1          0 IN- OUT OPAMP_MACRO
******* Main circuit ends here **************

******* Opamp macro model begins here **************
.SUBCKT OPAMP_MACRO    IN+ IN- OUT
Eb          N3 0 N2 0 1
Cb          0 N2  1.1n
VOS          N4 IN- 1m
Ro          OUT N3  75
Rid          IN+ N4  2MEG
Ed          N1 0 IN+ N4 1E5
Rb          N2 N1  16MEG
.ENDS
******* Opamp macro model ends here **************

******** Analysis begins here****************
.TRAN  0.05MS  2MS
.PROBE
.END
******** Analysis ends here***************
```

Problem: 2.79

1. The schematic for this problem is shown below



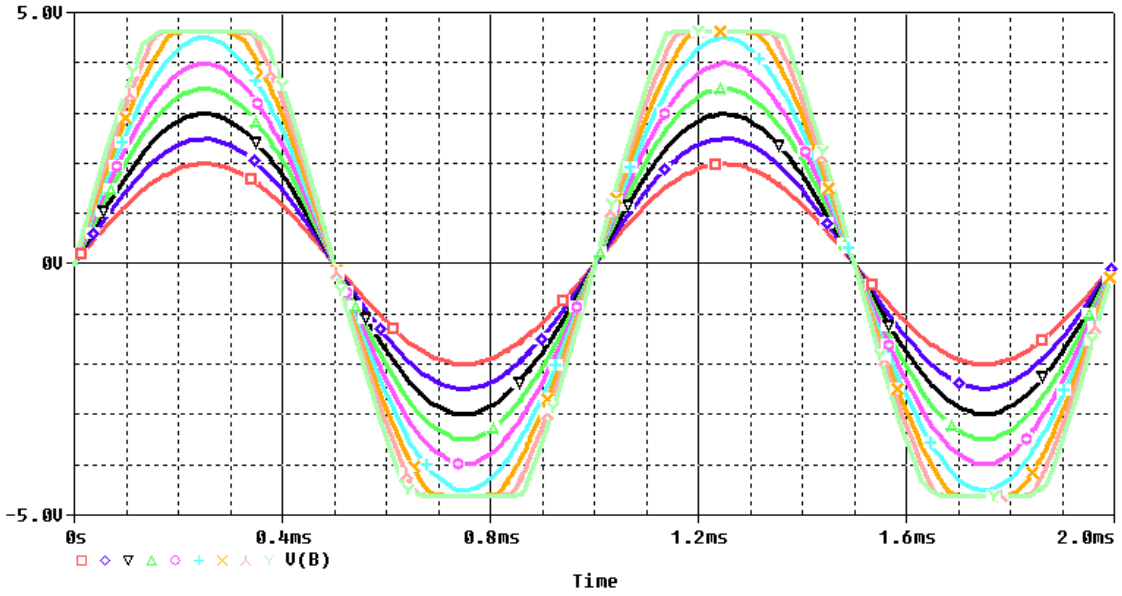
2. For part (a), run the netlist to perform a transient analysis. Plot V(B), V(C), and the difference between V(B) and V(C). The input waveform V(A) and the output V(B)-V(C) are plotted below



3. For Part (b), divide the peak to peak voltage of the output by the input to get the gain. The gain is 5 V/V.
4. For part (c) set up a parameter sweep which sweeps the value of input amplitude while measuring the output. An example, is shown below where the input amplitude is swept from 1 V to 3 V in steps of 0.25 V. The step size may be reduced for more accuracy. To perform this analysis, uncomment the following line in the analysis section.

```
*.STEP LIN PARAM AMPL 1 3 0.25
```

5. Plot the voltage V(B) as shown below to find out the input amplitude at which it starts clipping.



6. The output starts to clip when the input amplitude is above 2.25 V.

Netlist:

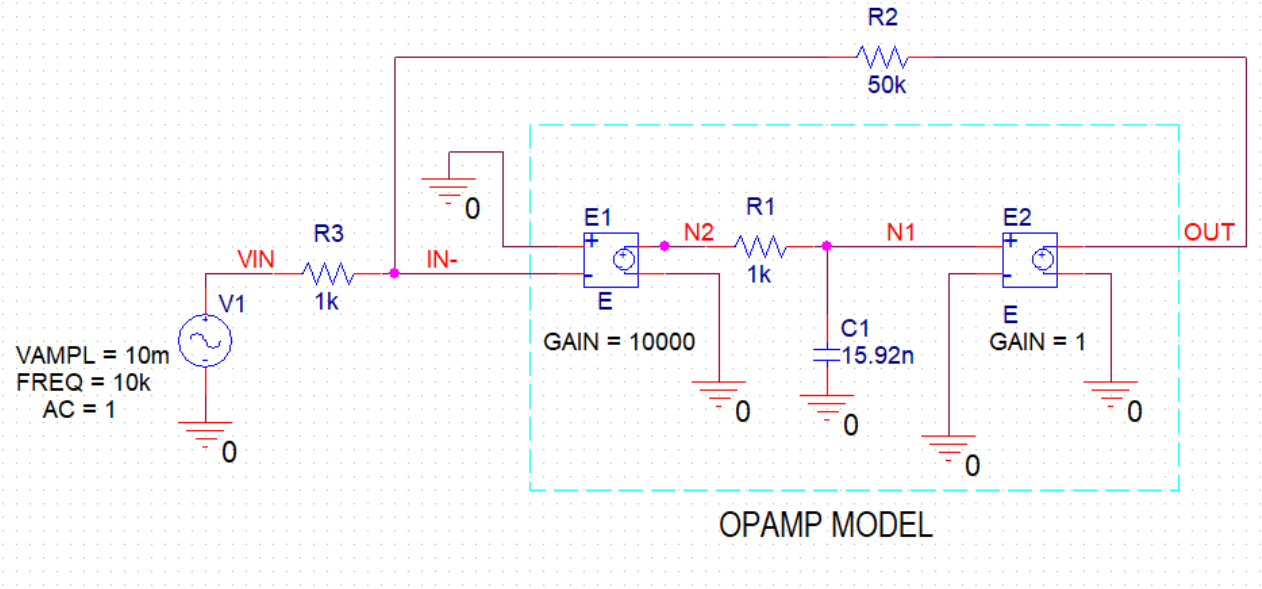
Copy the netlist given below and paste it into a text file and save it with *.cir extension.

```
********Problem: P2_79         ***************
******* Main circuit ends here **************
R5          N3 C  20k
R3          0 N1  10k
V1          A 0
+SIN 0 {AMPL} 1000 0 0 0
X_U1          N2 N1 VCC VEE B uA741
R4          N1 B  10k
X_U2          N4 N3 VCC VEE C uA741
VEE          0 VEE 5V
R2          A N2  10k
R6          0 N4  10k
VCC          VCC 0 5V
R1          A N3  10k
```

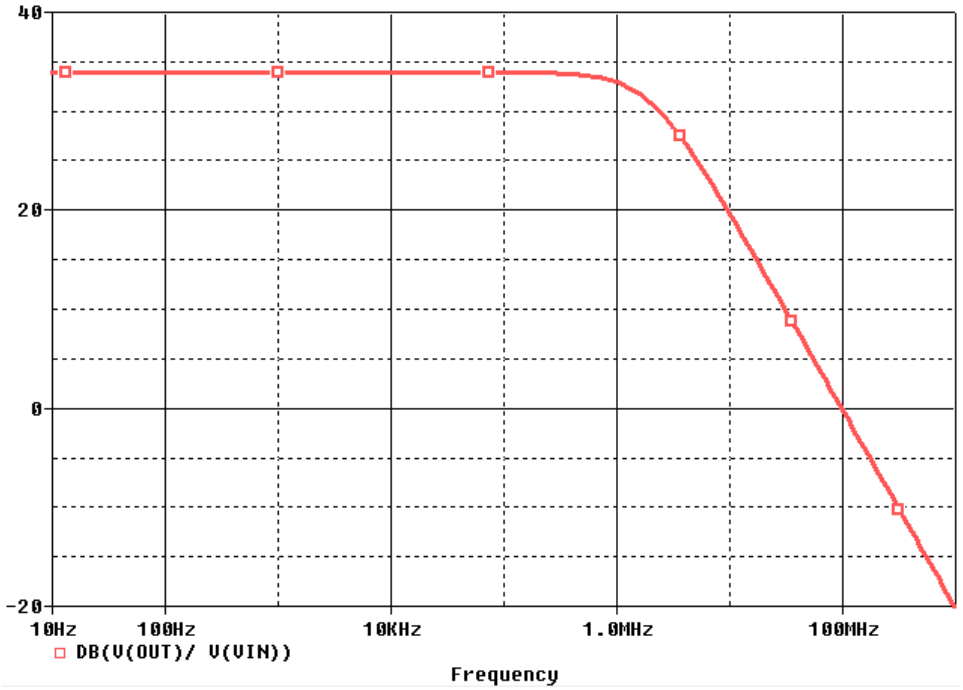
```
.PARAM  ampl=0.5
******** Model of uA741 begins here****************
* connections:   non-inverting input
*                |  inverting input
*                |  |  positive power supply
*                |  |  |  negative power supply
*                |  |  |  |  output
*                |  |  |  |  |
.subckt uA741    1 2 3 4 5
*
c1   11 12 8.661E-12
c2    6  7 30.00E-12
dc    5 53 dx
de   54  5 dx
dlp  90 91 dx
dln  92 90 dx
dp    4  3 dx
egnd 99  0 poly(2) (3,0) (4,0) 0 .5 .5
fb    7 99 poly(5) vb vc ve vlp vln 0 10.61E6 -10E6 10E6 10E6 -10E6
ga    6  0 11 12 188.5E-6
gcm   0  6 10 99 5.961E-9
iee  10  4 dc 15.16E-6
hlim 90  0 vlim 1K
q1   11  2 13 qx
q2   12  1 14 qx
r2    6  9 100.0E3
rc1   3 11 5.305E3
rc2   3 12 5.305E3
re1  13 10 1.836E3
re2  14 10 1.836E3
ree  10 99 13.19E6
ro1   8  5 50
ro2   7 99 100
rp    3  4 18.16E3
vb    9  0 dc 0
vc    3 53 dc 1
ve   54  4 dc 1
vlim  7  8 dc 0
vlp  91  0 dc 40
vln   0 92 dc 40
.model dx D(Is=800.0E-18 Rs=1)
.model qx NPN(Is=800.0E-18 Bf=93.75)
.ends
******** Model of uA741 ends here****************

******** Analysis begins here****************
.TRAN   0.05MS  2MS
*.STEP LIN PARAM AMPL 1 3 0.25
.PROBE
.END
******** Analysis ends here****************
```

Problem: 2.111

1. The schematic for this problem is shown below. The time constant of R1 and C1 is chosen to provide the specified unity-gain frequency.



2. Run the netlist to perform an AC Analysis for frequency range of 10 Hz to 10 GHz. Plot the magnitude response using the trace expression DB(V(OUT)/ V(VIN)) as shown below.



3. The 3-dB frequency f_{3dB} is at 1.96 MHz.
4. Measure the gain at $0.1f_{3dB}$ and 10 f_{3dB}.

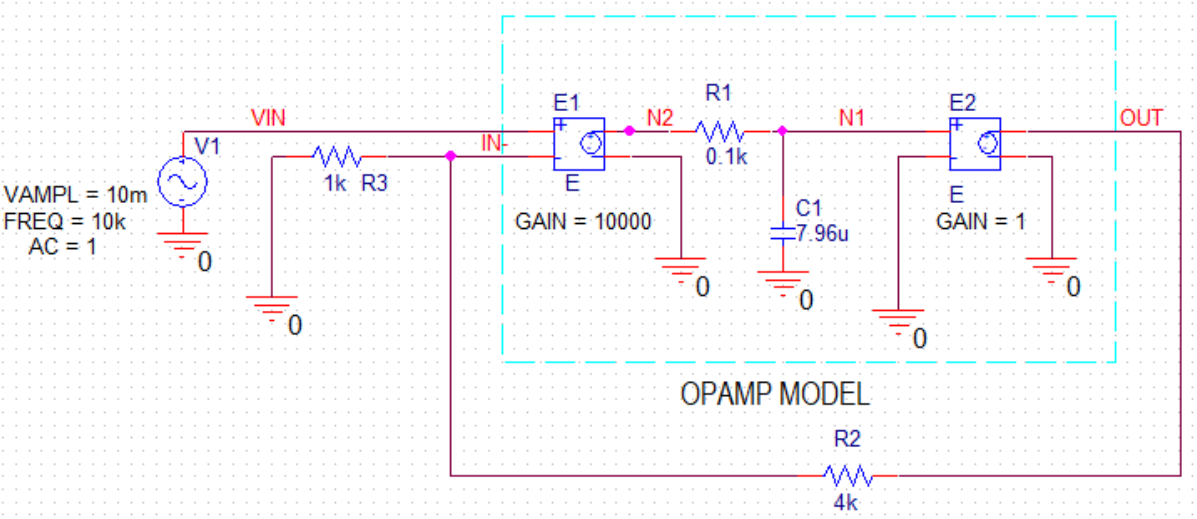
Netlist:

Copy the netlist given below and paste it into a text file and save it with *.cir extension.

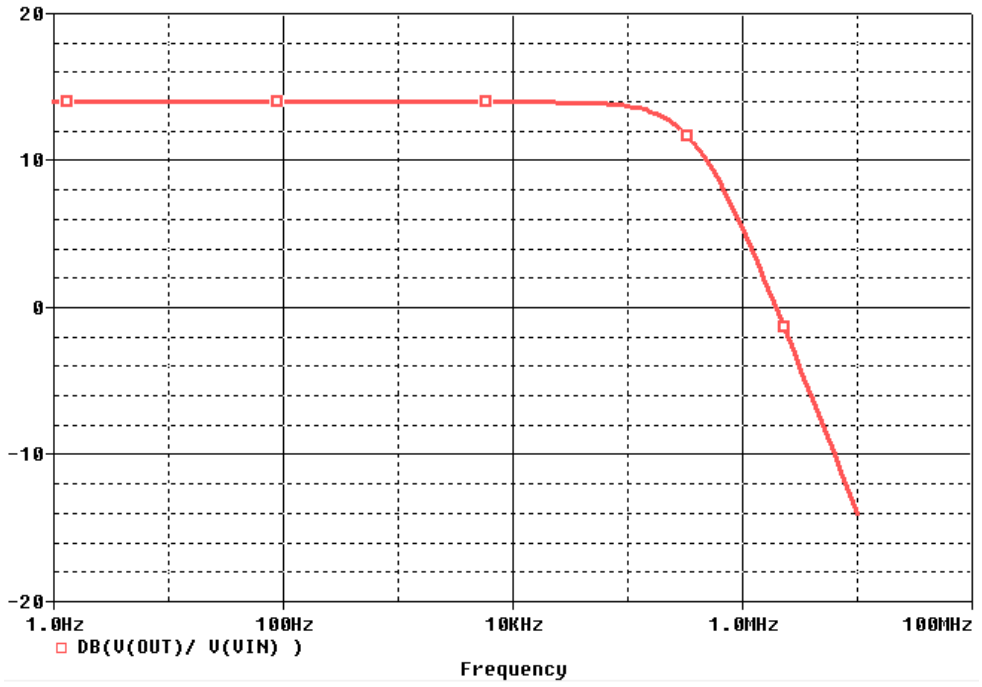
```
********Problem: P2_111       ***************
******* Main circuit begins here**************
E1          N2 0 0 IN- 10000
E2          OUT 0 N1 0 1
R1          N2 N1  1k TC=0,0
C1          0 N1  15.92n  TC=0,0
R2          IN- OUT  50k TC=0,0
R3          VIN IN-  1k TC=0,0
V1          VIN 0  AC 1
+SIN 0 10m 10k 0 0 0
******* Main circuit ends here **************

******** Analysis begins here****************
.AC  DEC   20  10 100G
.PROBE
.END
******** Analysis ends here****************
```

Problem: 2.115

1. The schematic for this problem is shown below. The time constant of R1 and C1 is chosen to provide the specified unity-gain frequency.

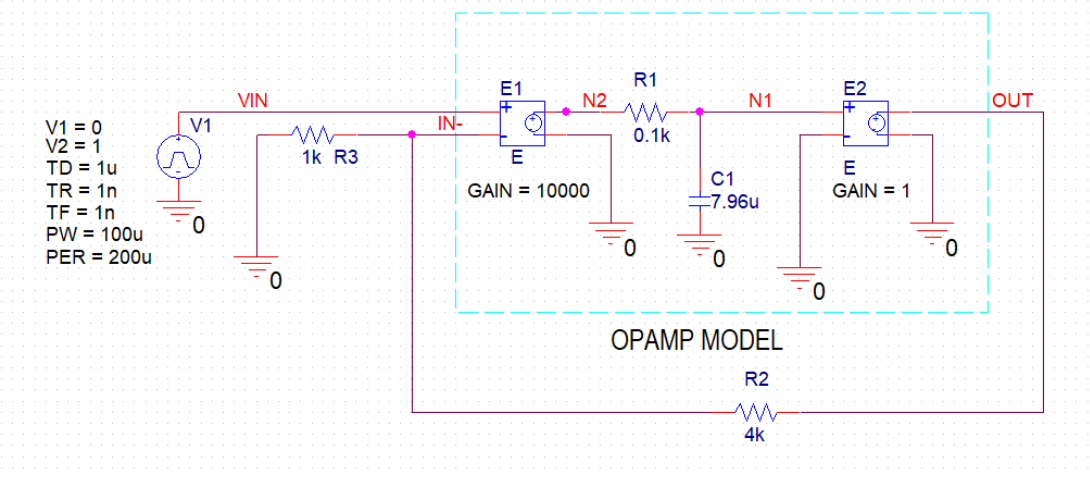


2. Run the netlist given below for AC Analysis for frequency range of 1 Hz to 10 MHz. And plot the gain using trace expression DB(V(OUT)/ V(VIN)) as shown below.



3. The 3-dB frequency f_{3dB} is at 400 kHz. The frequency at which gain is 1% below its low-frequency magnitude is at 56 kHz.
4. To perform the step response, use a VPULSE from the SOURCE to generate the step with the parameters shown below. In the netlist provided below, you may uncomment the VPULSE source and comment the VSINE source.

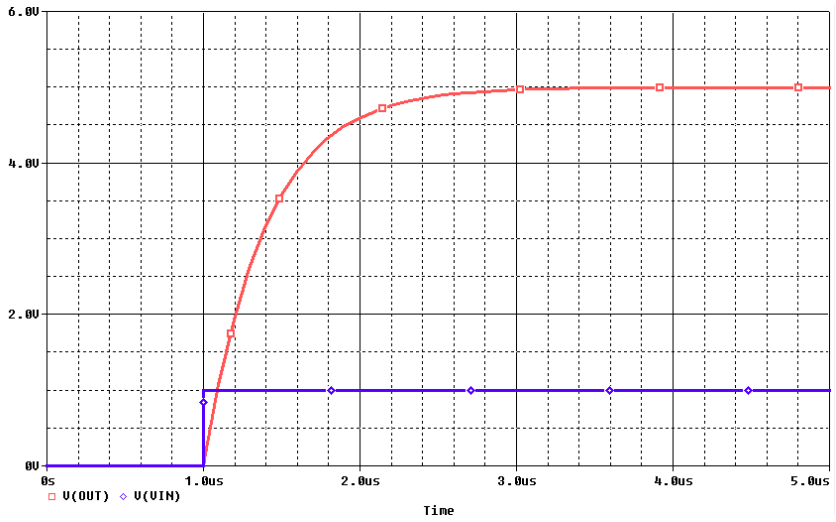
```
*+SIN 0 10m 10k 0 0 0
+PULSE 0 1 1u 1n 1n 100u 200u
```



5. Perform a transient analysis for a duration of 5 us by commenting the AC analysis command and uncommenting the transient analysis command.

```
*.AC   DEC    20   1  10MEG
.TRAN 0.005us 5us
```

6. Plot V(OUT) and V(IN) as shown above. To calculate the rise time of the output voltage going from 10% to 90%, use the cursor tool.



7. The rise time is 875 ns.

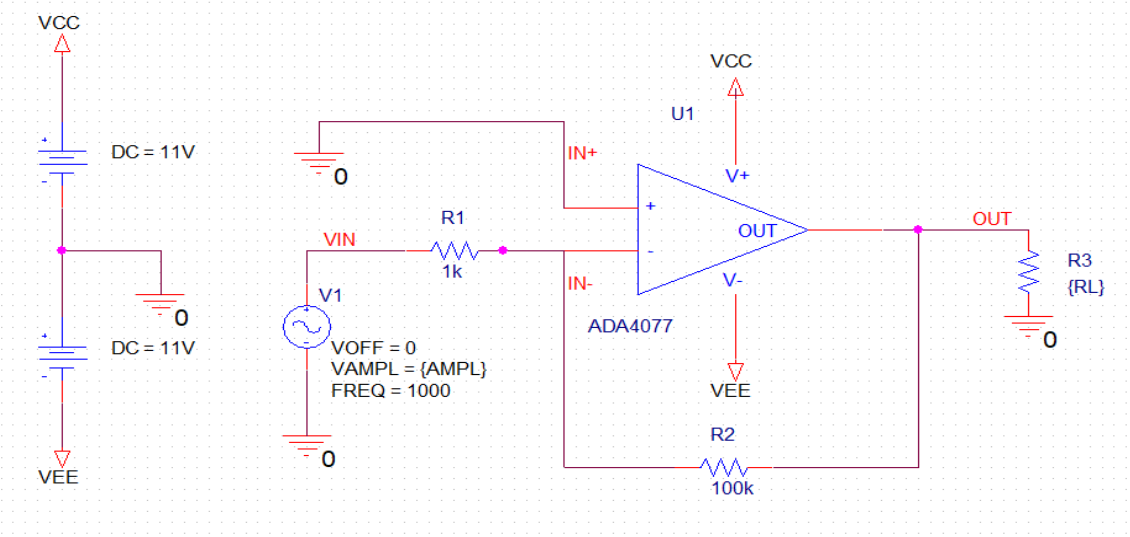
Netlist:

Copy the netlist given below and paste it into a text file and save it with *.cir extension.

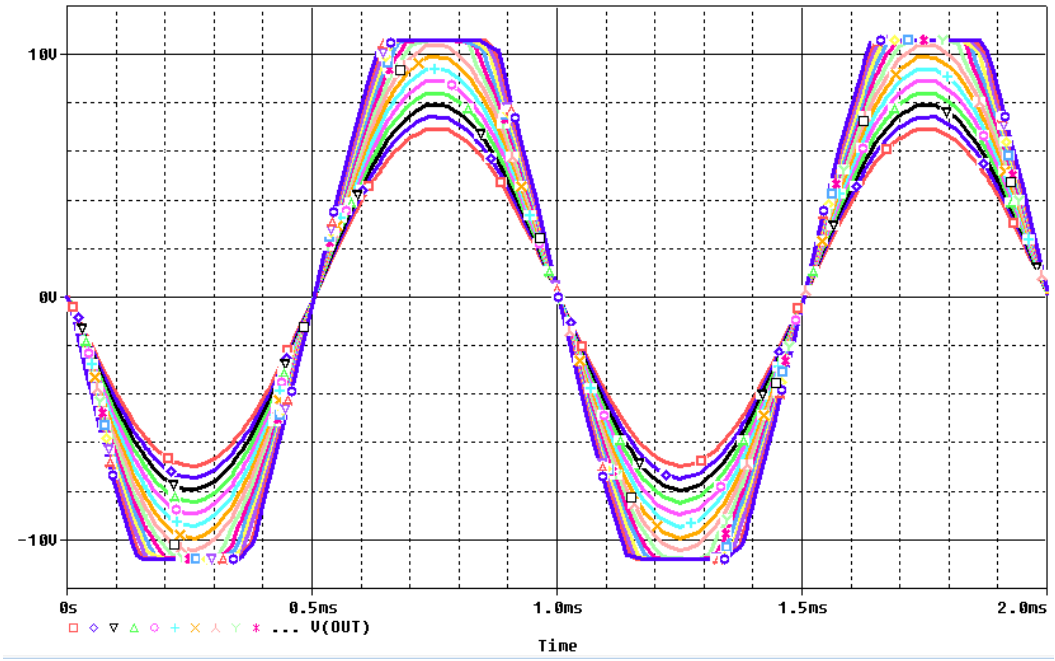
```
********Problem: P2_115               ***************
******* Main circuit begins here**************
C1          0 N1   7.96u  TC=0,0
R2          IN- OUT   4k TC=0,0
R1          N2 N1   0.1k TC=0,0
E1          N2 0 VIN IN- 10000
E2          OUT 0 N1 0 1
R3          0 IN-   1k TC=0,0
V1          VIN 0   AC 1
+SIN 0 10m 10k 0 0 0
*+PULSE 0 1 1u 1n 1n 100u 200u
******* Main circuit ends here **************

******** Analysis begins here****************
.AC   DEC    20   1 10MEG
*.TRAN 0.005us 5us
.PROBE
.END
******** Analysis ends here****************
```

Problem: 2.122

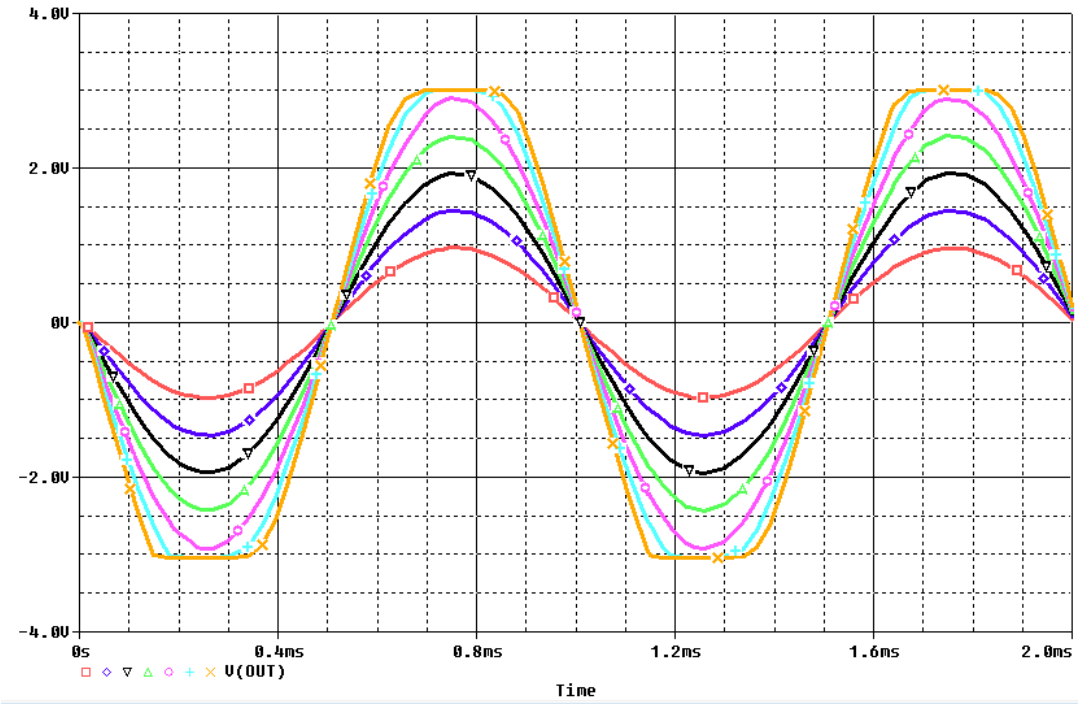
1. The schematic for this problem is shown below



2. For problem (a) run the netlist and perform a parametric transient analysis sweeping the amplitude of the input sine wave from 70 mV to 140 mV in steps of 5 mV. The resulting waveforms at the output V(OUT) are plotted below.



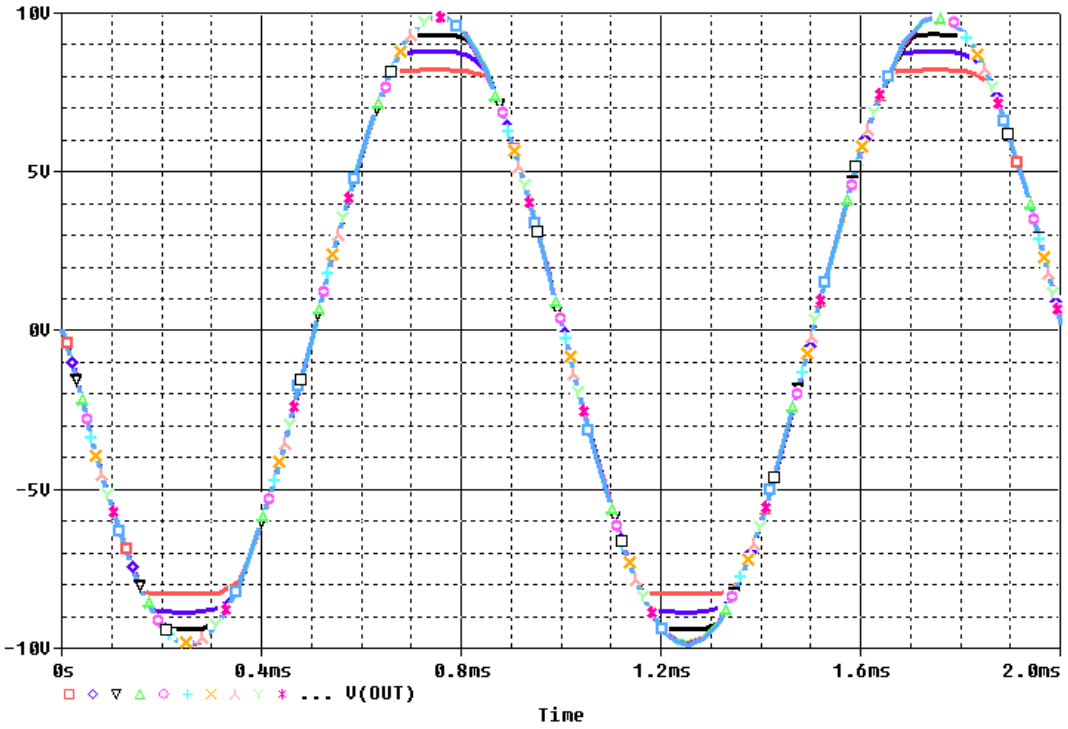
3. The maximum amplitude of the input without saturation at the output is 105 mV and the corresponding output has a peak amplitude of 10.44 V.
4. For problem (b), change the value of RL to 200 Ω. And perform the parametric simulation again sweeping the input amplitude from 10 mV to 40 mV in steps of 5 mV. The resulting output waveforms are plotted below



5. The maximum output peak amplitude has reduced to 2.92 V. The corresponding input amplitude is 30 mV.
6. For part (c), do a parametric analysis sweeping RL from 600 Ω to 1.1 kΩ in steps of 50 Ω. In this case the amplitude of the input voltage is set to its default value of 100 mV. To do this analysis comment the parametric analysis for the change in input amplitude and uncomment the change in RL.

```
*.STEP  LIN            PARAM   AMPL    70m     140m     5m
.STEP   LIN            PARAM   RL              600     1.1k     50
```

7. The waveform plotted at the output is shown below. The saturation voltage goes to a peak amplitude of 10 V when R3 is 800 Ω.



Netlist:

Copy the netlist given below and paste it into a text file and save it with *.cir extension.

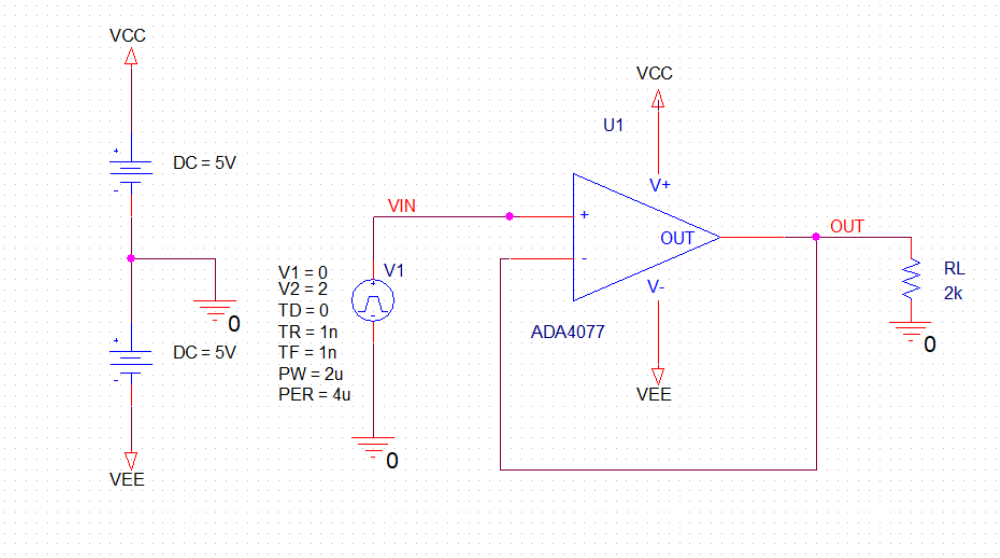
```
********Problem: P2_122                ***************
******* Main circuit begins here**************
VEE             0                VEE     11V
VCC             VCC              0               11V
V1              VIN              0
+SIN            0                {AMPL}  1000    0 0 0
X_U1          0           IN-     VCC     VEE             OUT     ADA4077
R1          VIN           IN-     1k              TC=0,0
R2          IN-           OUT     100k     TC=0,0
R3          0             OUT     {RL}            TC=0,0
.PARAM          AMPL=100m
.PARAM          RL=2k
******* Main circuit ends here **************

******** Model of ADA4077 begins here****************
* ADA4077 SPICE DMod model Typical values
* Description: Amplifier
* Generic Desc: 30V, BIP, OP, Low Noise, Low THD, 2X
* Developed by: RM ADSJ
* Revision History: 1.0 03/31/2015 - Updated to new header style
* 0.0 (11/2012)
* Copyright 2008, 2012,2015 by Analog Devices
*
* Refer to "README.DOC" file for License Statement.  Use of this
* model indicates your acceptance of the terms and provisions in
* the License Statement.
```

```
*
* Node Assignments
*                       noninverting input
*                       |       inverting input
*                       |       |       positive supply
*                       |       |       |       negative supply
*                       |       |       |       |       output
*                       |       |       |       |       |
.SUBCKT ADA4077         1       2       99      50      45
*
*INPUT STAGE
*
Q1   15 7 60 NIX
Q2   6 2 61 NIX
IOS  1 2 1.75E-10
I1  5 50 77e-6
EOS  7  1 POLY(4) (14,98) (73,98) (81,98) (70,98)  10E-6 1 1 1 1
RC1  11 15 2.6E4
RC2  11 6 2.6E4
RE1 60 5 0.896E2
RE2 61 5 0.896E2
C1   15 6 4.25E-13
D1  50 9 DX
V1  5  9 DC 1.8
D10 99 10 DX
V6 10 11 1.3
*
* CMRR
*
ECM   13 98 POLY(2) (1,98) (2,98) 0 7.192E-4 7.192E-4
RCM1  13 14 2.15E2
RCM2  14 98 5.31E-3
CCM1  13 14 1E-6
*
* PSRR
*
EPSY 72 98 POLY(1) (99,50) -1.683 0.056
CPS3 72 73 1E-6
RPS3 72 73 7.9577E+1
RPS4 73 98 6.5915E-4
*
* EXTRA POLE AND ZERO
*
G1 21 98 (6,15) 26E-6
R1 21 98 9.8E4
R2 21 22 9E6
C2 22 98 1.7614E-12
D3 21 99 DX
D4 50 21 DX
*
* VOLTAGE NOISE
*
VN1 80 98 0
RN1 80 98 16.45E-3
HN  81 98 VN1 6
RN2 81 98 1
*
* FLICKER NOISE
*
D5 69 98 DNOISE
VSN 69 98 DC .60551
H1 70 98 VSN 30.85
RN 70 98 1
```

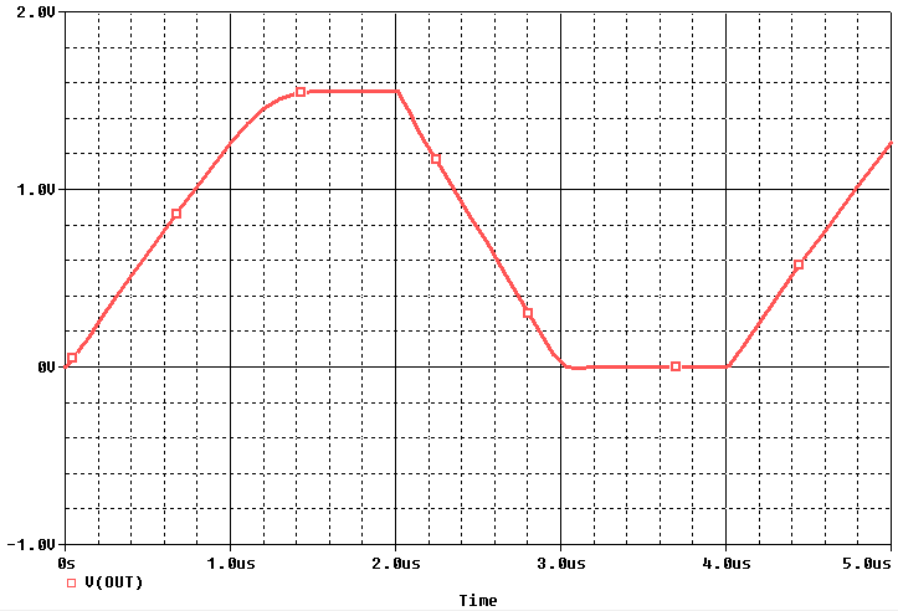
```
*
* INTERNAL VOLTAGE REFERENCE
*
EREF 98  0 POLY(2) (99,0) (50,0) 0 .5 .5
GSY  99 50 POLY(1) (99,50) 130E-6 1.7495E-10
*
* GAIN STAGE
*
G2  98 25 (21,98) 1E-6
R5  25 98 9.9E7
CF  45 25 2.69E-12
V4 25 33 5.3
D7 51 33 DX
EVN 51 98 (50,99) 0.5
V3 32 25 5.3
D6 32 97 DX
EVP 97 98 (99,50) 0.5
*
* OUTPUT STAGE
*
Q3   45 41 99 POUT
Q4   45 43 50 NOUT
RB1  40 41 9.25E4
RB2  42 43 9.25E4
EB1  99 40 POLY(1) (98,25) 0.7153  1
EB2  42 50 POLY(1) (25,98) 0.7153  1
*
* MODELS
*
.MODEL NIX NPN (BF=71429,IS=1E-16)
.MODEL POUT PNP (BF=200,VAF=50,BR=70,IS=1E-15,RC=71.25)
.MODEL NOUT NPN (BF=200,VAF=50,BR=22,IS=1E-15,RC=29.2)
.MODEL DX D(IS=1E-16, RS=5, KF=1E-15)
.MODEL DNOISE D(IS=1E-16,RS=0,KF=1.095E-14)
.ENDS ADA4077
*$
******** Model of ADA4077 ends here****************
******** Analysis begins here****************
.TRAN   0.05MS  2MS
.STEP   LIN             PARAM   AMPL    70m     140m     5m
*.STEP  LIN             PARAM   RL              600     1.1k     50
.PROBE
.END
******** Analysis ends here****************
```

Problem: 2.123

1. The schematic for this problem is shown below

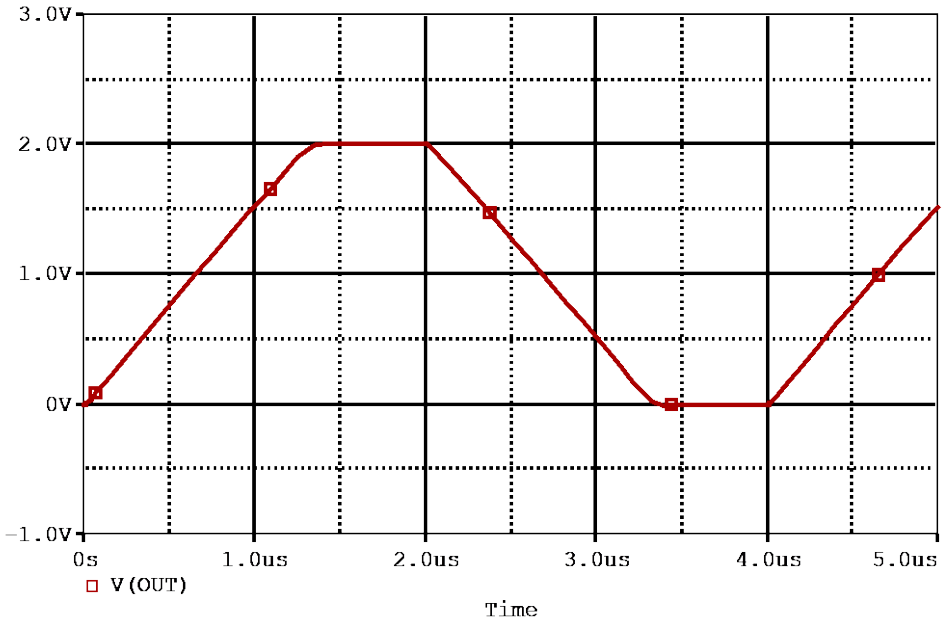


2. Run the netlist and perform the transient analysis for a duration of 5 us. A plot of the output V(OUT) is shown below.



3. Note that the output does not reach 2 V. This is because, with ±5V supplies, the output voltage range of the ADA4077 is insufficient. Increase the supply voltages to ±6V and see the following

result.



4. It takes around 1.4 us to reach 2 V. So, the shortest pulse should be more than this.

Netlist:

Copy the netlist given below and paste it into a text file and save it with *.cir extention.

```
********Problem: P2.123                ***************
******* Main circuit begins here**************
VEE          0 VEE 5V
VCC          VCC 0 5V
X_U1          VIN OUT VCC VEE OUT ADA4077
V1          VIN 0
+PULSE 0 2 0 1n 1n 2u 4u
RL          0 OUT  2k TC=0,0
 ******* Main circuit ends here **************

******** Model of ADA4077 begins here****************
* ADA4077 SPICE DMod model Typical values
* Description: Amplifier
* Generic Desc: 30V, BIP, OP, Low Noise, Low THD, 2X
* Developed by: RM ADSJ
* Revision History: 1.0 03/31/2015 - Updated to new header style
* 0.0 (11/2012)
* Copyright 2008, 2012,2015 by Analog Devices
*
* Refer to "README.DOC" file for License Statement.  Use of this
* model indicates your acceptance of the terms and provisions in
* the License Statement.
*
```

```
* Node Assignments
*                       noninverting input
*                       |       inverting input
*                       |       |       positive supply
*                       |       |       |       negative supply
*                       |       |       |       |       output
*                       |       |       |       |       |
*                       |       |       |       |       |
.SUBCKT ADA4077        1       2       99      50      45
*
*INPUT STAGE
*
Q1   15 7 60 NIX
Q2   6 2 61 NIX
IOS  1 2 1.75E-10
I1  5 50 77e-6
EOS  7  1 POLY(4) (14,98) (73,98) (81,98) (70,98)  10E-6 1 1 1 1
RC1  11 15 2.6E4
RC2  11 6 2.6E4
RE1 60 5 0.896E2
RE2 61 5 0.896E2
C1   15 6 4.25E-13
D1  50 9 DX
V1  5  9 DC 1.8
D10 99 10 DX
V6 10 11 1.3
*
* CMRR
*
ECM   13 98 POLY(2) (1,98) (2,98) 0 7.192E-4 7.192E-4
RCM1  13 14 2.15E2
RCM2  14 98 5.31E-3
CCM1  13 14 1E-6
*
* PSRR
*
EPSY 72 98 POLY(1) (99,50) -1.683 0.056
CPS3 72 73 1E-6
RPS3 72 73 7.9577E+1
RPS4 73 98 6.5915E-4
*
* EXTRA POLE AND ZERO
*
G1 21 98 (6,15) 26E-6
R1 21 98 9.8E4
R2 21 22 9E6
C2 22 98 1.7614E-12
D3 21 99 DX
D4 50 21 DX
*
* VOLTAGE NOISE
*
VN1 80 98 0
RN1 80 98 16.45E-3
HN  81 98 VN1 6
RN2 81 98 1
*
* FLICKER NOISE
*
D5 69 98 DNOISE
VSN 69 98 DC .60551
H1 70 98 VSN 30.85
RN 70 98 1
*
```

```
* INTERNAL VOLTAGE REFERENCE
*
EREF 98  0 POLY(2) (99,0) (50,0) 0 .5 .5
GSY  99 50 POLY(1) (99,50) 130E-6 1.7495E-10
*
* GAIN STAGE
*
G2  98 25 (21,98) 1E-6
R5  25 98 9.9E7
CF  45 25 2.69E-12
V4 25 33 5.3
D7 51 33 DX
EVN 51 98 (50,99) 0.5
V3 32 25 5.3
D6 32 97 DX
EVP 97 98 (99,50) 0.5
*
* OUTPUT STAGE
*
Q3   45 41 99 POUT
Q4   45 43 50 NOUT
RB1  40 41 9.25E4
RB2  42 43 9.25E4
EB1  99 40 POLY(1) (98,25) 0.7153  1
EB2  42 50 POLY(1) (25,98) 0.7153  1
*
* MODELS
*
.MODEL NIX NPN (BF=71429,IS=1E-16)
.MODEL POUT PNP (BF=200,VAF=50,BR=70,IS=1E-15,RC=71.25)
.MODEL NOUT NPN (BF=200,VAF=50,BR=22,IS=1E-15,RC=29.2)
.MODEL DX D(IS=1E-16, RS=5, KF=1E-15)
.MODEL DNOISE D(IS=1E-16,RS=0,KF=1.095E-14)
.ENDS ADA4077
*$
******** Model of ADA4077 ends here****************

******** Analysis begins here****************
.TRAN   0.05uS  5uS
.PROBE
.END
******** Analysis ends here****************
```